10

Device Series and Parallel Operation, Protection, and Interference

This chapter considers various areas of power device application that are often overlooked, or at best, underestimated. Such areas include parallel and series device utilisation, over-current and overvoltage protection, radio frequency interference (rfi) noise, filtering, and interactive noise effects.

10.1 Parallel and series connection and operation of power semiconductor devices

The power-handling capabilities of power semiconductor devices are generally limited by device area utilisation, encapsulation, and cooling efficiency. Many high-power applications exist where a single device is inadequate and, in order to increase power capability, devices are paralleled to increase current capability or series-connected to increase voltage ratings. Extensive series connection of devices is utilised in HVDC transmission thyristor and IGBT modules while extensive paralleling of IGBTs is common in inverter applications. Devices are also series connected in multilevel converters.

When devices are connected in series for high-voltage operation, both steady-state and transient voltages must be shared equally by each individual series device. If power devices are connected in parallel to obtain higher current capability, the current sharing during both switching and conduction is achieved either by matching appropriate device electrical and thermal characteristics or by using external forced sharing techniques.

10.1.1 Series semiconductor device operation

Owing to variations in blocking currents, junction capacitances, delay times, on-state voltage drops, and reverse recovery of individual power devices, external voltage equalisation networks and special gate circuits are required if devices are to be reliably connected and operated in series (or parallel).

10.1.1i - Steady-state voltage sharing

Figure 10.1 shows the forward off-state voltage-current characteristics of two power switching devices, such as SCRs or IGBTs. Both series devices conduct the same off-state leakage current but, as shown, each supports a different voltage. The total voltage blocked is \( V_1 + V_2 \) which can be significantly less than the sum of the individual voltage capabilities. Forced voltage sharing can be achieved by connecting a resistor of suitable resistance in parallel with each series device as shown in figure 10.2.

These equal value sharing resistors will consume power and it is therefore desirable to use as large resistance as possible. For worst case analysis consider \( n \) cells in series, where all the cells pass the maximum leakage current except cell \( D_1 \) which has the lowest leakage. Cell \( D_1 \) will support a larger blocking voltage than the remaining \( n - 1 \) which share voltage equally. Let \( V_c \) be the maximum blocking voltage for any cell which in the worst case analysis is supported by \( D_1 \). If the range of maximum rated leakage or blocking currents is from \( I_{1,s} \) to \( I_{2,s} \) then the maximum imbalance occurs when member \( D_1 \) has a leakage current of \( I_{1,s} \) whilst all the remainder conduct \( I_{2,s} \).

From figure 10.2, Kirchhoff’s current law at node ‘a’, gives

\[
\Delta I = I_2 - I_1 = I_2 - I_{1,s} \quad \text{(A)}
\]

where \( I_1 > I_2 \). The voltage across cell \( D_1 \) is

\[
V_{c1} = I_2 R \quad \text{(V)}
\]

By symmetry and Kirchhoff’s voltage law, the total string voltage to be supported, \( V_s \), is given by

\[
V_s = \frac{nV_c - V_0}{(n-1) I_{2,s}} \quad \text{ohms}
\]

for \( n \geq 2 \).

Generally only the maximum leakage current at rated voltage and maximum junction temperature is specified. By assuming \( I_s = 0 \), a conservative value of the maximum allowable resistance is obtained, namely

\[
R \leq \frac{nV_c - V_0}{(n-1) I_{1,s}} \quad \text{ohms}
\]
The extent to which \( nV_D \) is greater than \( V_a \) is termed the voltage sharing factor, namely
\[
k_x = \frac{V_a}{nV_D} \leq 1 \tag{10.7}
\]
As the number of devices is minimized the sharing factor approaches one, but equation (10.5) shows that undesirably the resistance for sharing decreases, hence losses increase.

The power dissipation of the resistor experiencing the highest voltage is given by
\[
P_D = \frac{V_n^2}{R} \tag{10.8}
\]
If resistors of ±10% per cent resistance tolerance are used, the worst case occurs when cell \( D_1 \) has a parallel resistance at the upper tolerance while all the other devices have parallel resistance at the lower limit. After using \( V_D = (1+a)I_aR \) and \( nV_D = (n-1)\cdot(1+a)I_aR + V_0 \) for equations (10.3) and (10.4), the maximum resistance is given by
\[
R = \frac{n(1-a)V_a - (1+a)V_a}{(n-1)(1-a^2)I_a} \tag{ohms} \tag{10.9}
\]
for \( n \geq 2 \).

The maximum loss in a resistor is
\[
P_D = \frac{V_D^2}{2R} \tag{10.10}
\]
If the dc supply tolerance is incorporated, then \( V_a \) in equations (10.6) and (10.9) is replaced by \((1+a)V_a\), where \( +100% \) is the supply percentage upper tolerance. This leads to a decreased resistance requirement, hence increased resistor power losses.
\[
R = \frac{n(1-a)V_a - (1+a)V_a}{(n-1)(1-a^2)I_a} \tag{ohms} \tag{10.11}
\]
The effects and importance of just a few per cent resistance or supply voltage tolerance on the maximum value for the sharing resistors and their power losses, are illustrated by example 10.1.

**Example 10.1:** Series device connection – static voltage balancing

Ten, 200 V reverse-blocking, ultra fast 35 ns reverse recovery diodes are to be employed in series in a 1500 V dc peak, string voltage application. If the maximum device reverse leakage current is 10 mA (at maximum junction temperature) calculate the voltage sharing factor, and for worst-case conditions, the maximum value of sharing resistance and power dissipation.

\[ i. \text{ If } 10 \text{ per cent tolerance resistors are employed, what is the maximum sharing resistance and its associated power rating?} \]
\[ ii. \text{ If a further allowance for supply voltage tolerance of } \pm 5\% \text{ is incorporated, what is the maximum sharing resistance and its associated power rating?} \]

**Solution**

When \( n = 10 \), \( V_a = 200 \text{ V dc} \), \( V_D = 1500 \text{ V dc} \), and \( I_a = 10 \text{ mA} \), the voltage sharing factor is
\[ k_x = 1500\text{V}/10\times200\text{VA} = 0.75 \]
Equation (10.6) yields the maximum allowable sharing resistance
\[
R = \frac{V_D - V_a}{I_a} = 5.53k\Omega
\]
The nearest (lower) preferred value, 4.7k\Ω, would be used.

Maximum resistor power losses occur when the diodes are continuously blocking. The maximum individual supporting voltage appears across the diode which conducts the least leakage current. Under worst case conditions this diode therefore supports voltage \( V_a \), hence maximum power loss \( P_D \) is
\[
P_D = \frac{V_a^2}{2R} = \frac{200^2}{4\times700\Omega} = 8.5\text{ W}
\]
Since the worse device, (in terms of sharing has least leakage current), is randomly located in the string, each 4.7k\Ω resistor must be capable of dissipating 8.5W.

The maximum 1500V dc supply leakage current is 42.5mA (10mA×1500V/10×4.7k\Ω) giving 63.8W total losses (1500V×42.5mA), of which 15W (10mA×1500V) is lost in the diodes.

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**Series and Parallel Device Operation and Protection**

10.1.1ii - Transient voltage sharing

When resistance tolerances are considered, sharing resistors of lower value must be used and the wider the tolerance, the lower will be the resistance and the higher the power losses. A number of solutions exist for reducing power losses and economic considerations dictate the acceptable trade-off level. Matched semiconductor devices would allow a minimum number of string devices (voltage sharing factor \( k_x = 1 \)) or, for a given string device number, a maximum number of sharing resistors (lowest losses). But matching is complicated by the fact that semiconductor leakage current varies significantly with temperature. Alternatively, by increasing the string device number (decreasing the leakage current), the sharing resistance requirement increases from 4.7k\Ω to 6.8k\Ω and resistor losses are reduced from a total of 50.8 W to 31 W. Another method of minimising sharing resistance losses is to minimise resistance tolerances. A tolerance reduction from 10 per cent to 5 per cent in example 10.1 increases the sharing resistance requirements from 1.8k\Ω to 3.9k\Ω, while total power losses are reduced from 140 W to 84 W. These worst case losses assume a near 100% off-state duty cycle.

10.1.iii - Transient voltage sharing

During steady-state or at very low frequencies, sharing resistors as shown in figure 10.2 are sufficient to prevent individual device overvoltage. Mismatching of turn-on delay times of thyristors and transistors can be minimised by supplying high enough turn-on drive with fast rise times. A higher initial dV/dt is then allowable. Before a conducting string of diodes or thyristors can reverse-block, reverse recovery charge must flow. Those elements with least recovery charge requirements recover first and support the reverse bias. The un-recovered devices recover slowly, since recovery now occurs as a result of the low leakage current though the recovered devices, and natural recombination. The transient reverse-blocking voltage can be shared more equally by placing capacitors across each string element as shown in figure 10.3. The capacitor action is to provide a transient current path bypassing a recovered device to allow a slower device to recover and to support voltage. In the case of thyristors, low value resistance is connected in series with each capacitor to avoid high capacitor discharge through the thyristors at turn-on. Figure 10.4 shows the \( I-V \) characteristics of two unmatched thyristors or diodes during reverse recovery.
Figure 10.3. A series diode string with shunting capacitance for transient reverse blocking voltage sharing.

Figure 10.4. Reverse recovery current and voltage for two mismatched series connected diodes.

The worst case assumptions for the analysis of figure 10.3 are that element D1 has minimum stored charge \( Q \) while all other devices have the maximum requirement, \( Q \). The charge difference is

\[ \Delta Q = Q - Q' \]  

(10.12)
The total string dc voltage \( V_n \) comprises the voltage across the fast-recovery device \( V_{o} \) plus the sum of each of the voltages across the slow \( n - 1 \) devices, \( V_{slow} \). That is

\[ V_n = V_o + (n - 1)V_{slow} \]  

(10.13)
The voltage across each slow device is given by

\[ V_{slow} = \frac{Q}{nQ} [V_o - \Delta V] \]  

(10.14)
Eliminating \( V_{slow} \) from equations (10.13) and (10.14) yields

\[ C \geq \frac{(n-1)Q}{nkV_o - V'} \]  

(10.15)
This equation shows that as the number of devices is minimized, the sharing factor, \( k_n \), which is in the denominator of equation (10.15), tends to one and the capacitance requirement undesirably increases.

Manufacturers do not specify the minimum reverse recovery charge but specify the maximum reverse recovery charge for a given initial forward current, reverse recovery di/dt, and temperature. For worst case design, assume \( Q = 0 \), thus

\[ C \geq \frac{(n-1)Q}{nkV_o - V'} \]  

(10.16)
Voltage sharing circuit design is complicated if the effects of reverse steady-state leakage current in ac thyristor blocking are taken into account.

Supply and sharing capacitance tolerances significantly affect the minimum capacitance requirement. Worst case assumptions for capacitance tolerances involve the case when the fastest recovering diode is in parallel with capacitance at its lower tolerance limit while all the other sharing capacitances are at their upper tolerance limit. Assuming the minimum reverse recovery charge is zero, then the minimum sharing capacitance requirement is

\[ C \geq \frac{(n-1)Q}{nkV_o - V'} \]  

(10.17)
where \(-10a\) is the capacitor negative percentage tolerance and \( n \geq 2 \). Voltage sharing resistors help minimise capacitor static voltage variation due to capacitance variations.

If the supply tolerance is incorporated, then \( V_s \) in equations (10.16) and (10.17) are replaced by \((1+b)V_o \) where \(+100\) is the supply percentage upper tolerance. This leads to an increased capacitance requirement, hence increased energy losses, \( \%CV_o^2 \).

\[ C \geq \frac{(n-1)Q}{(1-a)(nkV_o - (1+b)V')} \]  

(10.18)

Example 10.2: Series device connection – dynamic voltage balancing

The string of ten, 200 V diodes in worked example 10.1 is to incorporate capacitive reverse recovery transient sharing. Using the data in chapter 5, figure 5.9, specify a suitable sharing capacitance based on zero capacitance and supply tolerances \((a = b = 0)\), then \( \pm 10 \) per cent capacitance tolerances \((a = 0.1, b = 0)\), \pm 5 per cent supply tolerance \((a = 0, b = 0.05)\), then both tolerances \((a = 0.1, b = 0.05)\). Estimate in each case the capacitor energy loss at capacitor discharge.

Solution

Figure 5.9 shows that worst case reverse recovery conditions occur at maximum junction temperature, di/dt, and \( I_o \), and a value of \( Q = 6\mu F \) is appropriate.

The minimum possible sharing capacitance occurs when the capacitance and dc rail voltage are tightly specified. From equation (10.16)

\[ C \geq \frac{(n-1)Q}{nkV_o - V'} = \frac{(10-1) \times 6\mu F}{10 \times 200 V - 1500 V} \]  

(10.17)

The sharing capacitance requirement with 10% tolerance capacitors, is given by equation (10.17)

\[ C \geq \frac{(n-1)Q}{nkV_o - V'} = \frac{(10-1) \times 6\mu F}{10 \times 200 V - 1500 V} \]  

(10.17)

\[ C \geq \frac{(n-1)Q}{(1-a)(nkV_o - (1+b)V')} \]  

(10.18)
A further increase in capacitance requirement results if the upper tolerance dc rail voltage is used. From equation (10.18)

\[ C \geq \frac{(n-1)Q}{(1-a)(nkV_o - (1+b)V')} \]  

(10.17)
\[ = \frac{(10-1) \times 6\mu F}{(1-0.1)(10 \times 200 V - 1500 V)} \]  

(10.18)

In each tolerance case the next larger preferred capacitance value should be used, namely, 120nF, 120nF, and 150nF respectively, all rated at 200V dc.

The total series capacitance, using the upper tolerance limit is

\[ C_T = \frac{(1+a)C}{n} \]

The stored energy with a 1500V dc rail in the 10 series connect 150nF capacitors, and subsequently loss when the string voltages reduce to zero at diode forward bias, is therefore

\[ W = \frac{1}{2}CV_o^2 = \frac{1}{2} \left( \frac{1+a}{n} \right) V_o^2 \]  

(10.17)
\[ = \frac{1}{2} \left( \frac{1+0.1}{1} \right) \times 120nF \times 1500V^2 \times (1 + 0.05)^2 = 16.4mJ \]  

The energy stored in the 10 series connect 150nF capacitors, and subsequently loss when the string voltage reduces to zero at diode forward bias, is

\[ W = \frac{1}{2} \left( \frac{1+0.1}{1} \right) \times 150nF \times 1500V^2 \times (1 + 0.05)^2 = 20.5mJ \]  

(10.18)
When capacitive sharing is used with switching devices, at turn-on the transient sharing capacitor discharges into the switching device. The discharge current magnitude is controlled by the turn-on voltage fall characteristics. If a linear voltage fall at turn-on is assumed, then the transient sharing capacitor maximum discharge current is a constant current pulse for the fall duration, of magnitude

\[ I_{d} = C \frac{\Delta V}{\Delta T} \]  

(10.19)

The discharge current can be of the order of hundreds of amperes, incurring initial dv/dt values beyond the capabilities of the switching device. In example 10.2 the discharge current for a switch rather than a diode is approximately 150mA×200V/1µs =30A, assuming a 1µs voltage fall time. This 30A may not be insignificant compared to the switches current rating. But, advantageously, the sharing capacitors do act as turn-off snubbers, reducing switch turn-off stressing.

In the case of the thyristor, the addition of a low-valued, low inductance, resistor in series with each transient capacitor can control the capacitor discharge current, yet not significantly affect the transient sharing properties. The resultant R-C discharge current can provide thyristor latching current while still offering transient recovery sharing, dv/dt, and voltage spike suppression. Thyristor snubber operation and design are considered in chapter 8.1.2.

Figure 10.5 shows the complete steady-state and transient-sharing networks used for diodes, thyristors, and transistors. Transient voltage sharing for transistors involves the use of the conventional R-D-C snubber shown in figure 10.5c and considered in chapter 8. The series inductor used with thyristor and transistor strings provides transient turn-on voltage protection. The inductor supports the main voltage while each individual element switches on. Such an inductive turn-on snubber is mandatory for the GCT and the GTO thyristor. No one device is voltage-stressed as a consequence of having a longer turn-on delay time, although gate overdrive at turn-on minimises delay variations.

\[ I_{d} = \frac{V_{d}}{R} \]  

(10.20)

where

\[ V_{d} = \text{maximum allowable single device current rating} \]

\[ n = \text{number of parallel devices} \]

\[ k_{p} = \text{current parallel sharing factor} = I_{1}/nI_{m} \leq 1 \]

Parallel connection of IGBT die within a module is made possible by using die from the same wafer batch. On-state voltage matching for single large area wafers is expensive and complicated by the high temperature dependence of both static and dynamic electrical device characteristics. Derating does not account for effects such as layout and electrical and thermal impedance imbalance. The amount of derating is traded off against the extra cost involved in selecting devices with closer (matched) static characteristics.

\[ I_{n} = \max \text{current rating for each device} \]

(10.21)

Figure 10.6 shows the static I-V on-state characteristics of two SCRs. If these two devices are connected in parallel, for the same on-state voltage, the resultant current flow is \( I_{1} + I_{2} \), where \( I_{1} \) and \( I_{2} \) can be very different in value. The total current rating of the pair is not the sum of the maximum current rating for each but rather a value which can be just larger than the rating of one device alone. The percentage parallel derating \( p_{d} \) for \( n \) parallel connected devices is defined as

\[ p_{d} = \left( 1 - \frac{I_{n}}{nI_{m}} \right) \times 100 \]  

(10.22)

Forced current sharing is applicable to both steady-state and transient conditions. For a current derating of less than 5 per cent it is usually cheaper to use forced sharing techniques rather than matched devices.

\[ I_{n} = \max \text{discharge current for the fall duration} \]

(10.19)

From Kirchhoff's voltage law in figure 10.7

\[ V_{f} = V_{0} + I_{f}R = V_{0} + (I_{f} - I_{n})R \]  

From equation (10.20), rearranged for two devices, \( n = 2 \)

\[ I_{f} = 2(I_{1} - p_{d}I_{m}) \]

Substituting for \( I_{f} \) in equation (10.21) gives

\[ R = \frac{V_{0} - V_{f}}{2p_{d}I_{m}} \]  

(ohms)

(10.22)
For two devices; and (b) and (c) for many devices.

External forced current sharing networks using cross-coupled reactors: For worst case losses, $\delta \rightarrow 1$

$$\mathcal{P}_{D_{1}} = \delta \times I_{D_{1}} = 1 \times 100A = 100A$$

$$\mathcal{P}_{D_{2}} = \delta \times I_{D_{2}} = 1 \times 90A = 90A$$

$$I_{D_{1}} = \sqrt{\mathcal{P}_{D_{1}}} \times T_{D_{1}} = \sqrt{100} \times 100 = 100A$$

$$I_{D_{2}} = \sqrt{\mathcal{P}_{D_{2}}} \times T_{D_{2}} = \sqrt{90} \times 90 = 90A$$

$$P_{D_{1}} = I_{D_{1}} \times R_{D_{1}} = 100 \times 0.01 \Omega = 10W$$

$$P_{D_{2}} = I_{D_{2}} \times R_{D_{2}} = 90 \times 0.01 \Omega = 9W$$

$$P_{D_{12}} = P_{D_{1}} + P_{D_{2}} = 19W$$

For the two diodes shown in figure 10.6, with $I_{D_{1}} = 100A$ and $I_{D_{2}} = 90A$, the total losses are $\delta = 0.90$. The cell voltage drop is $1.6V + 100A \times 0.01 \Omega = 1.7V$. Thus, for an on-state duty cycle $\delta$, the total losses are $\delta \times 2.6V \times 190A = \delta \times 494W$.

Example 10.3: Resistive parallel current sharing – static current balancing

For the two diodes shown in figure 10.6, with $I_{D_{1}} = 100A$, what derating results when they are parallel connected, without any external sharing circuits? The maximum current rating for each device is $I_{m} = 100A$; hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.7 for current sharing, it is required that 100A flows through $D_{1}$ and 90A through $D_{2}$. Specify the per cent overall derating, the necessary sharing combination should be possible. Using the network in figure 10.7 for current sharing, it is required that 100A flows through $D_{1}$ and 90A through $D_{2}$. Specify the per cent overall derating, the necessary sharing combination should be possible.

For the most effective method of current sharing is to use coupled reactors as shown in figure 10.8. In these feedback arrangements, in figure 10.8a, if the current in $D_{1}$ tends to increase above that through $D_{2}$, the voltage across $D_{2}$ increases to oppose current flow through $D_{1}$. Simultaneously a negative voltage is applied to $D_{2}$, thereby increasing the voltage across $D_{2}$ thus increasing its current. This technique is most effective in ac circuits where the core is more readily designed to reset, avoiding saturation.
Equalising reactor arrangements are possible for any number of devices in parallel, as shown in figures 10.8b and c, but size and cost become limiting constraints. The technique is applicable to steady-state and transient sharing. At high current densities, the forward I-V characteristics of diodes and thyristors (and some IGBTs) have a positive temperature dependence which provides feedback aiding sharing.

The mean current in the device with the highest current, therefore lowest voltage, of \( n \) parallel connected devices in figure 10.8c (with one coupled circuit in series with each device), is given by

\[
\bar{I}_d = \frac{I_p}{n} \Delta V_d = \frac{I_p}{n} \left( \frac{v_{1s}}{n} \right) \Delta V_{ps} = \frac{I_p}{n} \left( \frac{\eta}{n} \right) \Delta V_{ps} t
\]

(10.26)

where \( \Delta V_{ps} \) is the maximum on-state voltage drop difference

\( \Delta V_s \) is the self-inductance (magnetising inductance) of the coupled inductor

\( T \) is the cycle period, \( 1/f \), and

\( r \) is the conduction period \( (r < T) \)

(a) current sharing analysis for two devices: \( r_s = 0 \)

Consider two thyristors \( (n = 2) \) connected in parallel as shown in figure 10.9. The coupled circuit magnetising current is modelled with the magnetising inductor \( L_M \). The transformer turns ratio is 1:1, hence the winding voltages and currents are equal, taking into account the relative winding flux orientation shown by the dots. Commutation inductance overlap is ignored.

From Kirchhoff's voltage law

\[
V_{f1} + V_1 = V_{f2} - V_2
\]

That is

\[
V_1 = V_{f2} - V_{f1} - V_L
\]

From Kirchhoff's current law

\[
I_p = I_1 - I_2
\]

From Faraday's equation

\[
V_{f1} = L_p \frac{di}{dt}
\]

which after integrating both sides gives

\[
I_p = \frac{1}{L_p} \int V_{f1} dt = \frac{1}{L_p} \Delta V_{ps} t
\]

(10.31)

As a condition it is assumed that the voltage difference \( \Delta V \) does not decrease as the operating point moves along the I-V characteristics. That is, both devices are modelled by \( v_1 = v_f + i x_r \), where the linear resistance \( r_s \) is zero, each have different zero current voltages that is different \( v_o \). \( \Delta V_o = \Delta V_r \). Actually \( D_1 \) moves further up the I-V characteristic with time as it conducts more current while \( D_2 \) moves towards the origin, as shown in figure 10.9b.

Figure 10.9. External forced current sharing network using cross-coupled reactors: (a) circuit (including magnetising inductance \( L_m \)) for two devices and (b) I-V operating points.

(b) current sharing analysis for two devices: \( r_s \neq 0 \)

If static resistance is included in the device model for current sharing analysis, then equation (10.30), assuming both devices have the equal resistance, becomes

\[
\Delta V_r = L_p \frac{di}{dt} + 2 \eta i_r
\]

(10.32)
Example 10.4: Transformer current sharing – static and dynamic current balancing

Two thyristors with the same forward conduction characteristics as the diodes in figure 10.6 are parallel connected using the coupled circuit arrangement in figure 10.8a. The maximum current rating for each device is \( I_{n} = 100A \); hence with suitable forced sharing a 190A combination should be possible. Using the network in figure 10.8a for current sharing, it is required that no more than rated current flow through the lower conducting voltage device, \( D_{1} \). Specify the per cent overall derating and the necessary sharing transformer properties assuming a half-wave, 180º conduction, phase-controlled, 50Hz, highly inductive load application.

What are the transformer core reset requirements?

Estimate inductance requirements if the thyristors have a static on-state resistance of 1mΩ.

Solution

As in example 10.3, the derating for the parallel situation depicted in figure 10.6, without external sharing, is

\[
\rho_d = \left[ 1 - \frac{170A}{2 \times 100A} \right] \times 100 = 15 \text{ per cent} \quad (k_p = 0.85)
\]

With forced transformer sharing, the objective derating is reduced from 15% to

\[
\rho_d' = \left[ 1 - \frac{190A}{2 \times 100A} \right] \times 100 = 5 \text{ per cent} \quad (k_p' = 0.95)
\]

When the two thyristors are turned on, the magnetizing current is assumed zero and transformer Tri increases and the associated thyristor current \( I_{1} \) increases, from equation (10.44), the opposing magnetising current in the other transformers reduces the associated device principal current.

The worst case conduction period in this ac application, giving maximum magnetising current, is for 180º conduction, that is, 10ms. Thus it is required that \( T_{1} \), the total current is 190A in total. From figure 10.6, the voltage difference between the thyristors, \( \Delta V_{1} \), is about 0.1V. Thus the transformer winding voltages will be 0.05V each, with polarities as shown in figure 10.9a. In time the magnetizing current increases and the current in \( T_{1} \) increases above 95A due to the increasing magnetizing current, while the current in \( T_{2} \) decreases below 95A, such that the total load current is maintained at 190A.

The worst case conduction period in this ac application, giving maximum magnetising current, is for 180° conduction, that is, 10ms. Thus it is required that \( T_{1} \) current rises to 100A and \( T_{2} \) current falls to 90A at \( t = 10ms \), that is, the magnetising current is 100A - 90A = 10A.

Substitution into equation (10.31) gives

\[
L = \frac{L_{2}}{n} \left[ 1 + \frac{\Delta V_{1}}{I_{n}} \right] \times 10ms = 50\mu H
\]

where it is assuming that the voltage differential \( \Delta V_{1} \) between the two devices is constant during the conduction period. In fact figure 10.9b shows that the voltage difference decreases, so assuming a constant value gives an under-estimate of requirements.

The core volt-µs during conduction is 0.05V×10ms = 500 V-µs. That is, during core reset the reverse voltage time integral must be at least 500 V-µs to ensure the core flux is reset, (magnetising current reduced to zero).

Using equation (10.34), with \( r_{n} = 1 \text{mΩ} \), gives

\[
L_{n} = \frac{n}{\Delta V_{1}} \left[ 1 + \frac{\Delta V_{1}}{I_{n}} \right] \times 10ms = 90\mu H
\]

The inductance, 50µH, given by equation (10.31) when neglecting model resistance, under-estimates requirements.
10.2 Protection Overview - over-voltage and over-current

All electrical systems are vulnerable to interference and damage from lightning or other short duration electrical surges or long supply system swells. As systems become more electronically complex, they also become more vulnerable to external and internally generated interference. A fault can be caused by a device failure or noise which results in undesired device turn-on. This will cause semiconductor device and equipment failure unless protective measures are utilised.

Protection against fault current effects usually involves fuses which clear in time to protect endangered devices, or transient absorption devices which absorb spike energy and clamp the equipment voltage. Dealing with over-voltage levels, the crowbar fault protection technique can be employed to divert the fault from sensitive components to the crowbar which is a robust circuit. The crowbar damps the sensitive circuit to zero volts and initiates an isolation breaker or fuse action.

An electrical surge is a temporary increase in voltage, current or both. The size, waveform, and form of the transient surge which can occur within a system are many and varied.

i. Lightning - A direct strike lightning current can potentially generate transients in the millions of volts and tens of thousands of amps, electronic equipment is rarely exposed to surges of this magnitude. The greatest exposure in power electronics systems is through interference and transmission lines. Domestic ac lines can carry voltage surges of up to 5kV and currents of the order of 1kA. Therefore, for the vast majority of instances where the chance of a lightning strike directly to the equipment is low, 5kV and 1kA is the limit of the direct strike or inductively generated surges. Exposed equipment, such as wind turbines, although suitable earthed, can experience significantly higher electrical surge stresses.

ii. Power Induction - Although power induction voltages can be high in voltage and current, they are often limited in duration. These voltages are caused by faults on the power system which couple into the system (usually inductively as a consequence of the surge causing a large fault current). In power transmission systems, these faults are quickly terminated by circuit breaker and re-closer equipment. This can occur in as short a cycle of powers of frequency, voltage, and rarely takes longer than a second. These transients are typically modelled as a 600V rms waveform lasting up to a second.

iii. Power Cross - Alternatively, power cross voltages are low voltage events but the exposure can occur over longer durations. They are often caused by safety audits or maintenance error or cabling faults and can result in moderate currents flowing for a longer period of time, for example, in domestic applications, 25A for 15 minutes. They are predominately at mains power supply voltage levels (100 to 220V rms).

iv. Earth Potential Rise (EPR) - EPR can be categorized into two forms:
   1. as a result of power system faults and
   2. lightning discharges.

In normal industry, where fault currents from the power system are limited in magnitude by fuses and circuit breakers, power system EPR is not usually a considerable risk. EPR only becomes a significant risk when power earthing systems are significantly below standard or where high power transmission systems are used such as at power generation and distribution facilities, within the high power industry, and in the vicinity of electrical traction systems (electric rail). Lightning EPR can only result from a direct strike to the building housing the equipment or in its immediate vicinity. Such events are unusual, unless the installation is particularly vulnerable due to location or extreme height (for example, wind turbine and cellular phone base-station antennae). The equipment exposure as a result of EPR can be high, and at high earth resistance locations, may become a significant portion of the lightning current.

Surge protection is the process of protecting electronic systems or equipment from voltages and currents which are outside their safe operating limits. These surge voltages and currents can be generated by short circuits, lightning or faults from a power system and usually enter the electronic system along inter-equipment wiring. The surges may be galvanically coupled into the system as in the case of a direct lightning strike, through an inadvertent connection of the power system to the wiring, or as a result of an earth potential rise. They may be capacitively coupled into the system which may occur when a data system is used in the vicinity of a high voltage power line. They may be inductively coupled into the system as may occur if the wiring is run in parallel with large lines carrying currents running in a power circuit feeding a high power motor. Such events can result in a wide variety of potential consequences.

Electrical surge protection performs several key functions:

- it must prevent or minimize damage caused by a surge;
- it must ensure the system returns to a working condition with minimal disruption to service;
- under normal conditions the protection must interfere with any signals or control circuitry, creating challenges for power electronics technologies;
- the protection must operate and fail in a safe predictable manner during overstress.

10.2.1 Ideal secondary level protection

Power electronic equipment is generally within a system that has primary protection, associated with the ac grid protection, for example. The installed equipment therefore may only require secondary protection. Secondary protection prevents the let-through energy of the primary protector (the energy of the surge that gets past the primary protector) from damaging the device.

The peak open circuit voltage of the let-through energy past the primary protector is smaller than the initial external surge. Therefore, a secondary protector can effectively block (series) and or divert (shunt) the reduced surge energy.

The requirements for this ideal blocking device are:

i. As the device needs to block the let-through energy of the primary protector, it can be a series component (in series with the transmission line), located just after the primary protector. As a series component, the device will react to the current through the device rather than, as with a shunt protector, voltage across the interface.

ii. A series device should have a predictable, stable and low trigger current (current at which the device changes between its conductive and non-conductive state) to provide effective protection for sensitive downstream equipment. A shunt device should operate (clamp or fold-back) at a level just above the maximum working voltage (but below device failure level).

iii. It should be fast acting (less than 10ns) to protect equipment from surges which rise at 5kV/µs - as with direct lightning strikes or lightning EPR.

iv. As a series device it should have low impedance (resistive, capacitive and inductive) so that it does not effect normal circuit operation, while for the same reasons, a shunt device should have a high standby impedance.

v. In the blocking mode, a series protector should have high impedance so that it does not dissipate significant energy during long duration surges, while for the same reasons, a shunt device should have a low clamping impedance.

vi. It should reset after the surge to reignite the system and continue to allow normal system operation.

vii. Re-set to normal after an incident, returning the equipment to pre-event operation.

viii. Debatably, after excessive stress, a shunt device should fail-safe open circuit, while a series device should failure short-circuit, so as to enable continued unprotected operation, but system protection is afforded.

In addition, for practical and economic reasons it should be small in size, light in weight, and low in cost.

Electrical protection devices fall into two key categories: over-voltage (usually shunt connected) and over-current (usually series connected). Over-voltage devices divert or shunt surge current produced by an over-voltage (such as lightning), as shown in Figure 10.11, while most over-current devices increase in resistance to possibly becoming open-circuit to limit the surge current flowing from longer duration surge currents (50/60 Hz power fault), as shown in the parts of figures 10.12.

There are two types of voltage limiting protectors: switching devices (gas discharge tube GDT and thyristor) that conduct (open-voltage fold-back) the line, and voltage clamping devices (metal oxide varistor MOV and transient voltage suppressor TVS). The waveforms of figure 10.11 highlight that switching devices result in lower stress levels than clamping devices (shaded area) for protected equipment during their operation. Functionally, all voltage protectors reset after the surge, while current protectors may or may not reset, depending on their operating mechanisms. For example, PTC thermistors are resettable; fuses are non-resettable.

Figure 10.11. Two shunt voltage control mechanisms, namely voltage clamping and voltage fold-back by switching action, with source and load voltages shown.
10.2.2 Overvoltage protection devices

Gas Discharge Tubes (GDT) create a quasi short circuit across the line when the internal gas is ionized by an overvoltage, returning to a high impedance state after the surge has ceased. These robust devices have the highest impulse current capability of any technology, and combined with negligible capacitance, make them attractive for the protection of high-speed digital and ac switching converter applications. Thyristor-based devices initially clamp the line voltage, and then switch to a low voltage on-state. After the surge, when the current drops below the holding current, the protector recovers and returns to its original high impedance blocking state. Transient Voltage Suppressors (TVS) or Zener diodes operate by rapidly moving from a high impedance to a non-linear resistance characteristic that clamps surge voltages. TVS diodes provide a fast-acting and controlled clamping voltage, however they have high capacitive and low energy capability which restricts the maximum surge current. Electrostatic discharge (ESD) devices clamping protectors consists of multilayer varisters (MLV) designed to protect equipment against ESD conditions. They have low leakage currents that make the devices transparent under normal operation. ESD transients cause the device to clamp the voltage by reducing its effective resistance and it resets to a high impedance state after the disturbance. Diode arrays for ESD protection combine thin film on silicon wafer fabrication technology and chip scale packaging. Such devices are used in portable electronic applications where a particular electrical response characteristic is specified for a minimum volume.

Figure 10.12. Three current limiting mechanisms: (a) current flow interruption, (b) current reduction, and (c) current diversion.

10.2.3 Over-current protection devices

Polymer Positive Temperature Coefficient (PTC) Thermistor resettable fuses are used in circuit current protection applications. Under high-current fault conditions, its resistance increases by many orders of magnitude and remains in a tripped state, continuing to provide continuous circuit protection until the fault is removed. Then after the power is cycled, the device returns to its normal low-resistance, low-loss state. Traditional fuses are constructed from a metal element encapsulated in a ceramic housing. The fuse element heats up at the rate related to $I^2R$. When the metal element temperature exceeds its melting point, it vaporizes and opens the circuit. The low resistance and losses of fuses are attractive for ac applications. Line Protection Modules (LPM) are based on a basic form of current protection: the Line Feed Resistor (LFR), normally fabricated as a thick-film resistor on a ceramic substrate. LPMs can withstand high-voltage impulses without breaking down. AC current interruption results when the high temperature developed by the resistor produces mechanical expansion stresses that cause the ceramic to break

A concise overview of generally available over-voltage and over-current protection devices is presented in Table 10.1. The following sections will consider each technology in detail.

Table 10.1: Overview of over-current and over-voltage protection devices and technologies

<table>
<thead>
<tr>
<th>Device</th>
<th>Over-voltage</th>
<th>Over-current</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDT</td>
<td>voltage switching</td>
<td>shunt</td>
</tr>
<tr>
<td>Thyristor</td>
<td>voltage switching</td>
<td>shunt</td>
</tr>
<tr>
<td>MOV</td>
<td>voltage clamping</td>
<td>shunt</td>
</tr>
<tr>
<td>TVS</td>
<td>voltage clamping</td>
<td>shunt</td>
</tr>
</tbody>
</table>

10.3 Over-current Protection

Current limiting devices provide a slow response, and are primarily aimed at protection from surges lasting hundreds of milliseconds or more, including power induction or contact with AC power. By combining a fixed resistor in series with a resettable protector, an optimum balance of nominal resistance and operating time is obtained. The inherent resistance of certain over-current protectors can also be useful in coordination and discrimination between primary and secondary overvoltage protection.

Positive Temperature Coefficient (PTC) Thermistors

Heat generated by current flowing in a PTC thermistor causes a step function increase in resistance towards an open circuit, gradually returning close to its original value once the current drops below a threshold value. The resistance stability after surges over time is a key aspect for preserving line balance. PTCs are commonly referred to as resettable fuses, and since low-level current faults are also be useful in coordination and discrimination between primary and secondary overvoltage protection.

Fuses

A fuse heats up during surges, and once the temperature of the metallic element exceeds its melting point, the normal low resistance creates an open circuit. The low resistance of fuses is attractive for power applications, but their operation is relatively imprecise and time-dependent. Once operated, they do not reset. Fuses also require additional resistance for primary coordination.

Since overvoltage protection usually consists of establishing a low impedance path across the equipment input, overvoltage protection itself will cause high currents to flow. Although relatively slow acting, fuses play a safety role in removing longer-term faults that would damage protection circuitry, thus reducing the size and cost of other protection elements. It is important to consider the I-t performance of the selected fuse, since even multiples of the rated current may not cause a fuse to rupture except after a significant delay. Coordination of this fuse behaviour with the I-t performance of other protection is critical to ensuring that there is no combination of current-level and duration for which the protection is ineffective. By including structures intended to rupture under excess current conditions or separate components, it is also possible to produce hybrid fusible resistors.

Heat Coils

Heat coils are thermally activated mechanical devices connected in series with the line being protected, which divert current to ground. A series coil operates a parallel shunt contact, typically by melting a solder joint that is restraining a spring-loaded contact. When a current generates enough heat to melt
the joint, the spring mechanically forces two contacts together, short-circuiting the line. Heat coils are added against ‘sneak currents’ that are too small to activate other methods. Their high inductance makes them unsuitable for digital lines. It is also possible to construct current interrupting heat coils which open the circuit as a result of over-current.

**Line Feed Resistors**

A Line Feed Resistor (LFR) is the most fundamental form of current protection, normally fabricated as a thick-film device on a ceramic substrate. With the ability to withstand high voltage impulses without breaking down, AC current interruption occurs when the high temperature developed by the resistor causes mechanical expansion stresses that result in the ceramic breaking open.

Low current power induction may not break open the LFR, creating long-term surface temperatures of much lower than 250°C. To avoid heat damage to the adjacent components, the maximum surface temperature can be limited to about 250°C by incorporating a series thermal fuse link on the LFR. The link consists of a solder alloy that melts when high temperatures occur for 10 seconds or more periods. Along with the high precision needed for balanced lines, LFRs have significant flexibility to integrate additional resistors, multiple devices, or even different protection technology within a single component. One possible limitation is the need to dimension the LFR to handle the resistive dissipation under surge conditions. Along with combining multiple non-inductive thick-film resistors on a single substrate to achieve matching to <1%, a resistor can be combined with other devices to optimize their interaction with the overall protection design. For example, a simple resistor is not ideal for protecting a wire, but combining a low value resistor with another over-current protector provides closer protection and less dissipation than either device can offer alone. Both functions can be integrated onto a single thick-film component using fusible elements, PTC thermistors, or thermal fuses. Similarly, more complex hybrids are available, adding surface mount components such as thyristor protectors, to produce coordinated sub-systems.

**Thermal Switches**

These switches are thermally activated, non-resetting mechanical devices mounted on a voltage-limiting device (normally a GDT). There are three common activation technologies: melting plastic insulator, melting solder pellet or a disconnect device. Melting occurs as a result of the temperature rise of the voltage-limiting device’s thermal overload condition when exposed to a continuous current flow. When the switch operates, it shorts out the voltage-limiting device, typically to ground, conducting the surge current previously flowing through the voltage limiting device.

- A plastic-melting based switch consists of a spring with a plastic insulator that separates the spring contact from the metallic conductors of the voltage limiting device. When the plastic melts, the spring contacts both conductors and shorts out the voltage limiting device.

- A solder-melting based switch consists of a spring mechanism that separates the line conductor from the ground conductor by a solder pellet. In the event of a thermal overload condition, the solder pellet melts and allows the spring contacts to short the line and ground terminals of the voltage-limiting device.

- A ‘snap action’ switch typically uses a spring assembly that is held in the open position by a soldered stand-off and will short out the voltage-limiting device when its switching temperature is reached. When the soldered connection melts, the switch is released and shorts out the line and ground terminals of the voltage limited device.

10.3.1 Protection with fuses

It is not economical to design a circuit where fault overloads are catered for by using devices and components which will withstand worst-case faults. A fuse link is normally used for circuit fault current protection. A fuse link is a current sensitive device designed to serve as the intentional weak link in the protective sub-systems. The current fuse link consists of a solder alloy that melts when high temperatures occur for 10 seconds or more periods. Along with the high precision needed for balanced lines, LFRs have significant flexibility to integrate additional resistors, multiple devices, or even different protection technology within a single component. One possible limitation is the need to dimension the LFR to handle the resistive dissipation under surge conditions. Along with combining multiple non-inductive thick-film resistors on a single substrate to achieve matching to <1%, a resistor can be combined with other devices to optimize their interaction with the overall protection design. For example, a simple resistor is not ideal for protecting a wire, but combining a low value resistor with another over-current protector provides closer protection and less dissipation than either device can offer alone. Both functions can be integrated onto a single thick-film component using fusible elements, PTC thermistors, or thermal fuses. Similarly, more complex hybrids are available, adding surface mount components such as thyristor protectors, to produce coordinated sub-systems.

A series L-R circuit can be used to model the prospective fault. The current characteristic is given by

$$I_L = \frac{\sin(\omega t - \phi) - \sin(\omega t - \phi)}{\sin(\omega t - \phi) - \sin(\omega t - \phi)}$$

(10.51)

where $\varphi$ is the angle of the short circuit, after the zero voltage cross-over, $\frac{\pi}{2} \leq \varphi \leq \pi$. Differentiation of equation (10.51) gives the current $\frac{dI}{dt}$, and the maximum initial $\frac{dI}{dt}$ is

$$\frac{dI}{dt} = \frac{\sin(\omega t - \phi)}{\sin(\omega t - \phi)}$$

(10.52)

This equation shows that the maximum initial $\frac{dI}{dt}$ occurs for a short circuit occurring at the peak of the ac supply, $\varphi = \frac{\pi}{2}$, and is independent of the circuit R-L, which is independent of $\varphi$.

The load fault energy, for a fuse link resistance $R$, is

$$W_L = \frac{1}{2} R \int_0^T I^2 dt$$

(3)

If the load current, shown in figure 10.13a, during fuse action is assumed to be triangular, then the clearing integral of the fuse is

$$W_L = \frac{1}{2} I^2 R \int_0^T t dt$$

(3)

If the resistance $R$ is assumed constant (because of its low resistivity temperature co-efficient), the value of $T$ $(\omega L)^{1/2}$ is proportional to the energy fed to the protected circuit. The $I^2 R$ term is called the total let-through energy or the virtual clearing integral of the fuse. The energy which melts the fuse is proportional to $\frac{1}{2} I^2 R$, and is termed the pre-arcing or melting $I^2 R$. [Figure 10.13. The current fuse link: (a) a 50 A 650 V ac fuse link and (b) a silver fuse link element.]
Chapter 10
Series and Parallel Device Operation and Protection

10.3.1i - Pre-arcing $I^2t$
Before a fuse melts, the fuse is affected only by the current flowing. The pre-arcing or melting $I^2t$ characteristics of fuse links are therefore only a function of prospective fault current and are independent of voltage. For melting times longer than 5 to 10 ms, the time-current characteristics are usually used for design. Typical time-current characteristics for four different current rated fuses are shown in figure 10.15. For times less than a millisecond, the melting $I^2t$ reduces to a minimum and the pre-arcing $I^2t$ characteristics shown in figure 10.16 are most useful. The peak let-through current $I_p$ is a function of prospective fault current $I_a$ for a given supply voltage. Typical current cut-off characteristics are shown in figure 10.17.

10.3.1ii - Total $I^2t$ let-through
For fuse operating times of less than about 10 milliseconds the arcing $I^2t$ can be considerably larger than the pre-arcing $I^2t$ and it varies considerably with system voltage, fault level, power factor, and the point on the wave when the fault is initiated. The higher the voltage the more onerous is the duty of the fuse link because of the increase in energy absorbed by the fuse link during the arcing process. Under short-circuit conditions this leads to an increase in $I^2t$ let-through with voltage. The $I^2t$ let-through will decrease with increased supply frequency whereas the cut-off current will increase. The peak arc voltage after melting is usually specified for a given fuse link type and is a function of supply voltage, as indicated by the typical arcing voltage characteristics in figure 10.18. The faster the fault is cleared, the higher the arc voltage $V_a$. Typical total $I^2t$ let-through values for total operating times of less than 10 ms, at a given voltage, are shown in figure 10.19. Derating factors for temperature, frequency, and power factor are shown in figure 10.20.

10.3.1iii - Fuse link and semiconductor $I^2t$ co-ordination
Difficulties arise in matching fuses with semiconductors because each has very different thermal and electrical properties. Semiconductor manufacturers publish (mainly for diodes and thyristors) $I^2t$ withstand values for their devices for times less than 10 ms. To ensure fuse link protection the total $I^2t$ let-through by the fuse link under appropriate circuit conditions should be less than the $I^2t$ withstand ability of the semiconductor.
Fuse link manufacturers usually give the data shown in figures 10.15 to 10.20. In ac applications the parameters on which the semiconductor withstand capability is normally compared to the fuse link are

- Peak let-through current versus clearing time or clearing \( I^2t \)
- Applied voltage
- Power factor

![Figure 10.17. Fuse-link cut-off characteristics at 660 V rms.](image)

![Figure 10.18. Typical peak arc voltage for two different fuse-link types.](image)

The voltage rating indicates that the fuse can be relied upon to safely interrupt its rated short circuit current in a circuit where the voltage is equal to, or less than, its rated voltage. The standard voltage ratings used by fuse manufacturers for most small dimension and midget fuses are 32, 63, 125, 250 and 600. In electronic equipment with relatively low output power supplies, with circuit impedance limiting short circuit currents to values of less than ten times the current rating of the fuse, it is common practice to specify fuses with 125 or 250 volt ratings for secondary circuit protection of 500 volts or higher.

10.3.1iv – Fuse link derating and losses

For 25ºC ambient temperatures, it is recommended that fuses be operated at no more than 75% of the nominal current rating established using the controlled test conditions. Fuses are essentially temperature-sensitive devices whose ratings have been established in a 25ºC ambient. Even small variations from the controlled test conditions can greatly affect the predicted life of a fuse when it is loaded to its nominal value, usually expressed as 100% of rating.

To compensate for variable operating factors, for trouble-free, long-life fuse protection of equipment, the fuse should not be used at more than 75% of the nominal rating, whilst ensuring overload and short circuit protection must be adequately provided for. The fuse temperature generated by the current passing through the fuse increases with increased ambient temperature. Increased ambient temperature decreases the nominal current rating of a fuse. Most traditional fuse designs use lower melting temperature materials and are, therefore, more sensitive to ambient temperature changes.

The resistance of a fuse is usually an insignificant part of the total circuit resistance. Since the resistance of fractional amperage fuses can be several ohms, this fact should be considered when using them in low-voltage circuits. Most fuses are manufactured from materials which have positive temperature coefficients, and, therefore, it is common to refer to cold resistance and hot resistance (voltage drop at rated current), with actual operation being somewhere in between. Cold resistance is the resistance obtained using a measuring current of no more than 10% of the fuse's nominal rated current. Hot resistance is the resistance calculated from the stabilized voltage drop across the fuse, with current equal to the nominal rated current flowing through it.

The maximum permissible continuous fuse current \( I \) is dependant on the ambient temperature \( T_{amb} \) and the air flow velocity, according to

\[
I \leq I_{n} \times (1 - 0.005 \times (T_{amb} - 20^\circ C)) \times (1 + 0.05v) \times K_b
\]

where \( I_{n} \) is the fuse rated current and the air velocity, \( v \), is limited to 5m/s. The fuse load constant \( K_b \) is assumed worst case, that is 100% conduction, \( K_b = 1 \).
In the absence of manufacturer’s curves as in figure 10.20a, being a resistive element, fuse losses are related to the square of the current, that is

\[ P_{\text{loss}} = \left( \frac{\text{amps of } I}{1000} \right)^2 \times P_{\text{loss}} \]

where \( P_{\text{loss}} \) is the fuse losses at rated current \( I_n \) in a 20°C ambient.

Example 10.5: AC circuit fuse link design

A fast acting fuse is connected in series with a thyristor in a 415 V ac, 50 Hz ac application. The average current in the thyristor is 30 A at a maximum ambient temperature of 45°C. The ratings of the thyristor are

- \( I_{\text{TRMS}} = 45 \) A @ \( T_c = 85°C \)
- \( I_{\text{TRMS}} = 80 \) A
- \( I^2t = 5 \) kA²-s for 10 ms @ 125°C
- \( I^2t = 20 \) kA²-s
- \( I_{\text{TRMS}} = 1000 \) A for 10 ms @ 125°C and \( V_{\text{BASE}} = 0 \)

The fault circuit inductance is 1.32 mH and the resistance is negligible. Using figures 10.15 to 10.20, select a suitable fuse.

Solution

From figure 10.20a, the 35 A rms No. 2 fuse is rated at 30 A rms in a 45°C ambient.
From figure 10.18 the peak ac voltage for a type No. 2 fuse will be less than 1200 V, hence the thyristor voltage rating must be greater than 1200 V and possibly 1200V+√2×415 V, depending on the point-on-wave of the fault and the particular circuit configuration.
The following example illustrates the application of $I^2t$ for a fusing undergoing repetitive surges.

**Example 10.6: AC circuit fuse link design for $I^2t$ surges**

Based on figures 10.16 and 10.21, select a 230V, very fast-acting fuse that is capable of withstanding 100,000 pulses of current having a triangular pulse waveform of 20A magnitude and of 3ms duration. The normal operating current is 4.5A at an ambient temperature of 25ºC.

**Solution**

At 25ºC, no fuse thermal derating is necessary. The first waveform and the associated effective pulse $I^2t$ formula in figure 10.21 are applicable, where $i_p = 20A$ and the effective duration is 3ms.

The applicable value for peak pulse current $i_p$ and time $t$ into the corresponding formula for the first wave-shape in figure 10.21 gives:

$$I^2t = \frac{22}{22} \times 0.40A \times 3ms = 1.82A^2s$$

This value is referred to as the pulse $I^2t$.

The required nominal melting $I^2t$ value for 100,000 occurrences of the calculated pulse $I^2t$ from figure 10.22, involves a derating figure of 22%. The calculated pulse $I^2t$ is converted to the necessary nominal melting $I^2t$ values as follows:

$$Nominal\ Melt\ 22\% = 0.4 = 1.82\ A^2s$$

Examine the $I^2t$ rating data for a 230V, very fast-acting fuse. From figure 10.16, the 6A design is rated at $2A^2s$, which is the minimum fuse rating that will accommodate the 1.82A^2s value calculated. This 6A fuse will also accommodate the specified 4.5A normal operating current, when a 25% derating factor is applied to the 6A nominal rating.

**10.3.1vi - Other fuse link derating factors**

**Ambient temperature correction coefficient, $A_1$**

Fuse current ratings are usually established at a reference ambient air temperature $T_{ref}$ of 25°C or 30°C. Typical ambient operating temperatures are greater, $T_{op}$, so the fuse must be derated. The temperature rise depends on the internal power dissipation, which is a function of the current squared. The derating coefficient, for a maximum allowable fuse temperature of $T_{max}$ (typically 130°C to 150°C), is

$$A_1 = \left( \frac{T_{max} - T_{op}}{T_{max} - T_{ref}} \right)$$

**Forced cooling correction coefficient, $B_1$**

Forced air cooling, up to a limit about $v=5m/s$, increases the fuse continuous rating by up to 25%, according to:

$$B_1 = 1 + 0.05 \times v \leq 1.25$$

**Terminal conductor size coefficient, $C_1$**

Connected cables and busbars conduct heat away from the fuse, thereby affecting the fuse temperature. A factor 0.8 to 1 can account for busbar conduction and the effects of nearby heat sources. Liquid cooling of the terminals can result in a correction factor of greater than one.

**High frequency derating coefficient, $C_f$**

The fuse link element is a metal strip, in which at fundamental frequencies $f$ above 1kHz, its resistance is increased by skin effects. The $I^2R$ losses are increased, where the current includes harmonics, which should not exceed 15% more than the fundamental. The derating is applicable from 100Hz up to 20kHz is shown in the following table. The function $C_f = 1 - 0.075 \times \log_{10} f$ may be applicable for certain fuses.
Current-variation coefficient $A_i$

Large rms variations cause thermal fatigue of the small notch zones on the fuse link used for semiconductor fuses. The thermal derating is classified as either continuous or cyclic.

On/off operation a few time per day with minimal overloads is considered continuous operation, and has an associated 20% derating, $A_i = 0.8$. Equipment turned on and off once per day, or less often, is fuse derated by 10%, $A_i = 0.9$.

Cyclic loading is when the fuse heats and cools to steady-state at a cycle rate of less than a few tens of minutes, $A_i \leq 0.6$.

The fuse current rating for a nominal current $I_n$ is derated to a maximum rms continuous current of

$$I_s = I_n \times A_i \times B_i \times C_i \times D_i \times E_i \times F_i$$

### Example 10.7: AC circuit fuse link derating

A 1000A fuse has following operational data:
- Reference temperature $T_{ref} = 30^\circ C$
- Modest busbars giving $C_i = 0.85$
- Forced air cooling velocity $v = 2m/s$

The operational environment is:
- Ambient temperature $T_a = 50^\circ C$
- Fundamental frequency $f = 1kHz$
- Cyclic operation: cyclic every hour, $A_i = 0.6$

What is the maximum allowable continuous current for the fuse?

#### Solution

From the frequency derating table $A_i = 0.9$ at 1kHz.

$$A_i = \left[ \frac{T_{ref} - T_a}{T_{ref} - T_{ref}} \right] / \left[ \frac{T_{ref} - T_{ref}}{T_{ref} - T_{ref}} \right] = 0.91$$

$$B_i = 1 + 0.05 \times v = 1 + 0.05 \times 2m/s = 1.1$$

$$C_i = 1 - 0.075 \times \log_{10} f$$

$$= 1 - 0.075 \times \log_{10} 1kHz = 0.775$$

The fuse adjusted rating is

$$I_s = I_n \times A_i \times B_i \times C_i \times D_i \times E_i \times F_i$$

$= 1000A \times 0.91 \times 1.1 \times 0.85 \times 0.9 \times 0.6 = 460A$

The adjusted rating of 460A is significantly lower than the 1000A applicable to rated fuse conditions.

### 10.3.1vii – Fuse link dc operation

Fuse link protection in dc circuits presents greater difficulty than for ac circuits. No natural ac period current zeros exist and faults can result in continuous arcing. The breaking capacity of a fuse link in a dc application depends on:

- the maximum applied dc voltage, $E$
- the feed $L/R$ time constant, $\tau$
- the prospective short-circuit current of the circuit, $I_s$

High-speed semiconductor ac fuses can be used in dc applications, after suitable derating. The longer the fault current $L/R$ time constant, the lower the allowable operating voltage, since the fuse takes longer to melt due to the slower energy delivery rate. Conversely, the higher the prospective short-circuit current $I_s$, the faster the fuse operates hence it can operate at a higher dc voltage level.

Typically, the fuse dc rating is 70% of its ac voltage rating for time constants between 10ms to 20ms, and the dc rating decreases as the time constant increases. No voltage derating is necessary for time constants less than 2.5ms.

Published fuse characteristics and performance data generally concentrate on ac at 50Hz or 60Hz values. The design monograph in figure 10.23 can be used to select a suitable ac high-speed fuse for dc application. The design requires the fault time constant $\tau = \frac{I_s}{L/R}$, which will specify the maximum allowable dc voltage $E$, whence the maximum ac arcing voltage $V_{ac}$. The fault time constant also specifies the pre-arching $I^2 \tau$ derating factor $k$, used to specify the minimum prospective fault current $I_f$ to ensure enough energy for the fuse to melt, hence clear.

$$I_f = k \sqrt{I_s \cdot \tau}$$

This minimum current must be less than the prospective peak dc fault current given by

$$I_s = \frac{E}{R}$$

That is, $I_f < I_s$ is a fuse link requirement.

The instantaneous fault current is $i(t) = I_f (1 - e^{-t/\tau})$, while the instantaneous rms current is

$$I_{rms}(t) = I_f \sqrt{1 + \frac{2 \omega^2}{n} - \frac{1}{n^2}}$$

where

- $n = \frac{\tau}{f}$, the number of time constants

$$\frac{E}{V_{ac}} = \frac{I_s}{I_f}$$

$$I_{rms}(t) = I_f \sqrt{1 + \frac{2 \omega^2}{n} - \frac{1}{n^2}}$$

![Figure 10.23](image-url)
Example 10.8: DC circuit fuse link design

A traction 600V dc supply has an equivalent source impedance of 20mΩ and 0.4mH, and a nominal dc load current of 600A.

i. Validate the suitability of the following ac fuse in being able to safely clear a dc fault current.

ii. Estimate the fuse losses at 20°C ambient.

iii. What is the maximum nominal current allowable in an air still 80°C ambient?

iv. Estimate the fuse losses in the 80°C ambient.

FUSE: High speed 900A, 1300V ac, with a pre-arching $I^2 t$ of 505,000A$^2$s at room temperature, in a case size #3 of cross section 75mm×76mm, allowing 125W of losses at 20°C.

Figure 10.23 is applicable to this fuse link element.

**Solution**

The maximum applied voltage is $\bar{E} = 600$ V dc

The short circuit fault current constant is $r = \sqrt{R/c_p} = 0.4\text{mH}/\sqrt{20\text{mΩ}} = 20\text{ms}$

i. From figure 10.23, a size #3 fuse will offer better voltage and current overheads than a type #2 fuse. The data yields $k = 36$, an arcing voltage maximum of 1920V dc, and would allow fault time constants of up to 30ms or peak dc supply voltages of up to 700V dc.

The prospective short circuit fault current from equation (10.57) is $I_s = \frac{E}{R} = 600V/20\text{mΩ} = 30kA$.

From equation (10.56), the minimum allowable fault current to ensure enough energy to melt and clear the fuse is 

$$ I_s = k \times \sqrt{I^2 t} $$

$$ = 36 \times \sqrt{505,000} = 25.6kA $$

Since $I_s < I_n$, that is, 25.6kA < 30kA, the fuse will reliably and predictably melt, thence clear.

ii. The 125W fuse loss at rated current of 900A is reduced if the nominal load current is 600A. From equation (10.55):

$$ P_{in} = \left(\frac{I_n}{I_n}\right) \times P_{nom} $$

$$ = \left(\frac{900A}{600A}\right) \times 125W = 55\% W $$

iii. At ambient temperatures above 20°C, the fuse nominal current rating is decreased according to equation (10.54):

$$ I \leq I_n \times \left[1 - 0.005 \times (T_{ambient} - 20°C)\right] \times \left(1 + 0.05 \times V \times D_t\right) $$

$$ \leq 900A \times \left[1 - 0.005 \times (80°C - 20°C)\right] \times \left(1 + 0.05 \times 0 \times 1\right) $$

$$ \leq 900A \times \left[1 - 0.005 \times 60°C\right] = 630A $$

Thus the fuse would be satisfactory at 80°C with the nominal load current of 600A dc.

iv. The fuse losses at 600A in an 80°C ambient would be approximately

$$ P = \left(\frac{I_n}{I_n}\right) \times P_{nom} $$

$$ = \left(\frac{630A}{900A}\right) \times 125W = 113W $$

10.3.iii. - Alternatives to dc fuse operation

It may be possible in some applications to use an ac fuse in a dc circuit, before the rectification stage. Generally low voltage fuses are more effective than high voltage fuses. In high voltage transformer applications satisfactory protection may be afforded by transferring the fuse to the low voltage side. The fuse $I^2 t$ rating is transferred as with impedance transferring, that is, in the turns ratio squared.

**10.3.ii. - Protection with resettable fuses**

Resettable fuses are basically thermistors. Thermistors are thermally sensitive resistors and have, according to type, a negative (NTC), or positive (PTC) resistance/temperature coefficient.

PTC (positive temperature coefficient) thermistors are ceramic or polymeric crystalline protection components whose electrical resistance rapidly increases as a certain temperature is exceeded. Over-current circuit protection can be accomplished with the use of either a traditional fuse-link or PTC device.

PTC devices are typically used in a wide variety of electronics applications where over-current events are common and automatic resettable is desired. This ability of a PTC device to reset itself after experiencing a fault current makes it ideal within circuits that are not readily accessible or where a constant uptime is required.

There are two types of PTC thermistors based on different underlying materials: polymer and ceramic, as summarised in Table 10.2. Generally the device cross-sectional area determines the surge current capability, and the device thickness determines the surge voltage capability.

**Thermal Properties**

The operation of all PTC devices is based on an overall energy balance described by equation (10.60), which assumes a uniform temperature distribution within the device:

$$ H \frac{dT}{dt} = I^2 R \times (T - T_a) $$

(10.60)

where

- $I = $current flowing through the device, A
- $R = $resistance of the device, $\Omega$
- $H = $heat capacity of the PTC thermistor device, J/$K$
- $m = $mass of the device, kg
- $c_p = $heat capacity of the PTC thermistor device, J/kg K
- $T_a = $ambient temperature, K
- $U = $effective heat-transfer coefficient, heat dissipation factor, $W/K$
- $V = $nominal voltage, $V$
- $D_t = $change in device temperature, K
- $t = $time, s
- $\Delta = $change in voltage, V
- $E = $energy, J

In equation (10.60), the current flowing through the device generates heat at a rate equal to $I^2 R$. All or some of this heat is lost to the environment, at a rate described by the term $U(h\times A)$. Any heat not lost to the environment raises the device temperature at a rate described by the term $m\times c_p\times H\times k\times T_a\times D_t\times D_t$. Any heat not lost to the environment raises the device temperature at a rate described by the term $m\times c_p\times H\times k\times T_a\times D_t\times D_t$.

The maximum applied voltage is $E = \bar{E} \times (1 - 0.05 \times V \times D_t\times D_t)$

(10.61)

Under normal operating conditions, this thermal steady-state is at a relatively low temperature and in the low resistance region, as indicated by operating Point 1 in Figure 10.24.

The thermal characteristics of PTC devices are similar to those of the NTC devices, and can be described by the following terms:

- heat capacity, $H$, in J/K
- heat dissipation constant, $D$, in W/K
- thermal time constant, $t$, in seconds

**Heat capacity**

The product of the specific heat and mass of the thermistor, heat capacity is the amount of heat required to produce a 1K change in the body temperature of the thermistor.

$$ H = m \times c_p $$

Ceramic PTC thermistors have a heat capacity of about 3.4J/cm$^3$/K.
Heat dissipation constant

The heat dissipation factor is the amount of heat which is lost, over a unit of time, based on a 1K temperature difference between the heating element and ambient temperature. It is the ratio of the change in the power applied to the thermistor to the resulting change in body temperature due to self-heating. The factors that affect the dissipation constant including lead-wire materials, method of mounting, ambient temperature, conduction or convection paths between the device and its surroundings, and the structure, shape, and material of the PTC device itself.

\[ P = IV = U(T - T_a) = U\Delta T \] (W)

\[ T: \text{temperature of heating element, K} \]
\[ U: \text{heat dissipation factor, W/K} \]

Thermal time constant

The time required for the thermistor to change 63.2% of the difference between the self-heated temperature and the ambient after the power is disconnected. The thermal time constant is also influenced by the same environmental factors as those that affect the dissipation constant.

\[ \tau = \frac{H}{U} \] (s)

\[ U: \text{heat dissipation factor, W/K} \]
\[ H: \text{heat capacity, J/K} \]

10.3.2 Polymeric PTC devices

Polymeric PTC materials

Polymeric positive temperature coefficient circuit protectors are made from a conductive plastic formed into thin sheets, with electrodes attached to either side of the compressed stacked sheets. The conductive plastic matrix is manufactured from a nonconductive crystalline polymer and dispersed highly-conductive black particles, typically high density polyethylene mixed with graphite. The plate electrodes ensure even distribution of power loss through the device, and provide a surface for leads to be attached or for surface mounting. The phenomena that allows conductive plastic materials to be used for resettable over-current protection devices is that they exhibit a large non-linear positive temperature coefficient effect when heated. A PTC is a thermal characteristic that many materials exhibit whereby resistance increases with temperature. What makes a PTC conductive plastic material unique is the magnitude of its resistance increase. At a specific transition temperature, the increase in resistance is so large that it is characterised on a logarithmic scale.

Resettable over-current polymeric PTC protector physics

The conductive carbon black filler material in the PTC device is dispersed in a polymer that has a crystalline structure. The crystalline structure densely packs the carbon particles into its crystalline boundary so they are close enough together (beyond a level called the percolation threshold) to allow current to flow through the polymer insulator via the created carbon "chains", due to a tunnelling effect. When the conductive plastic is at room temperature, there are numerous carbon chains forming parallel conductive paths through the mostly crystalline material.

Under electrical fault conditions, excessive current flows through the PTC device. Internal $I^\prime R$ Joule heating causes the conductive plastic material's temperature to rise. As this self-heating continues, the material's temperature increases to rise until it exceeds its phase transformation temperature. As the material passes through this phase transformation temperature, the densely packed crystalline polymer matrix changes to an amorphous structure, disrupting the network of conductive carbon paths. This phase change is accompanied by a small volumetric expansion. As the conductive particles move apart from each other, most of them no longer conduct current and the resistance of the device increases sharply.

The material will stay 'hot', remaining in this high resistance state as long as the power is applied. This latched state provides continuous forward protection, until the electrical fault is cleared and the power is reduced. Reversing the phase transformation, by cooling, allows the carbon chains to re-form as the polymer re-crystallizes. The resistance quickly reduces toward its original low value.

Principle of operation

Both polymeric positive temperature coefficient thermistor protectors and traditional fuse-link devices react to internal $I^\prime R$ Joule heat generated by an excessive current flow in a circuit. Whereas a fuse-link melts open, interrupting the current flow, a PTC device restricts current flow as its bulk rises in temperature, changing from a low to a high resistance state. In both cases, this transitional condition is termed tripping. The characteristic curve in figure 10.24 shows the typical response of a PTC device to temperature.

![Figure 10.24. Polymeric PTC thermistor operating R-V-I-t curves and typical tripping dispersion.](image)

If the current through the device is increased while the ambient temperature is maintained constant, the heat generated within the device increases and the temperature of the device also increases. Whilst the increase in current is modest, if the generated heat can be lost to the environment, the device will stabilize according to equation (10.61) at a higher temperature, such as Point 2 in Figure 10.24. Alternatively, instead of the current being increased, the ambient temperature is raised, the device will stabilize according to equation (10.61) at a higher temperature, possibly again at Point 2. Point 2 could also be attained by a combination of both a current increase and an ambient temperature increase.

Further increase in either current, ambient temperature, or both will cause the device to reach a temperature where the resistance begins to rapidly increases, such as at Point 3 in Figure 10.24. Any further increase in current or ambient temperature will cause the device to generate heat at a rate greater than the rate at which heat can be transferred to the environment, thus causing the device to heat up rapidly. A large increase in resistance occurs for a small change in temperature. In Figure 10.24, this region of large change in resistance for a small change in temperature occurs between points 3 and 4, and this operating region is termed the latched state. This large increase in resistance causes a corresponding decrease in the current flowing in the down-line series circuit.

The resultant current reduction reduces the likelihood of circuit damage. Since the temperature change between operating points 3 and 4 is small, the term $(T - T_a)$ in equation (10.61) can be replaced by the constant $(T_{op} - T_3)$, where $T_{op}$ is the operating temperature of the device. Then equation (10.60) becomes:

\[ I^\prime R = \frac{V^2}{R} = U \times (T_{op} - T_3) \] (W)

\[ R: \text{resistance, } \Omega \]
\[ V: \text{voltage, } \text{V} \]
\[ U: \text{voltage drop, } \text{A} \]
Since both \( U \) and \( (T_{op} - T_A) \) are now constants, equation (10.63) reduces to a constant, \( IR = \) constant; that is, the device now operates in a constant power state. Expressing this constant power as \( V^2/R \) emphasizes that, in the tripped state, the device resistance is proportional to the square of the applied voltage. This relation holds until the device resistance reaches the upper knee of the curve, Point 4 in Figure 10.24.

For a device that has tripped, as long as the applied voltage is high enough for the resulting \( V^2/R \) power to maintain the \( U(T_{op} - T_A) \) loss, the device remains in the tripped state, that is, the device will remain latched in its protective high-resistance state. When the tripped voltage is decreased to the point where the \( U(T_{op} - T_A) \) loss can no longer be supplied, the device begins to reset to a lower resistance state, by traversing back along the R-T characteristic towards Point 1.

### Electric Properties

The electrical characteristics describing PTC devices (ceramic and polymeric) include the following:
- current-time characteristic
- resistance-temperature characteristic
- voltage-current characteristic
- power and minimum resistance
- temperature coefficient of resistance
- transition temperature
- voltage and frequency dependence
- voltage rating

### Hold and trip current

Figure 10.25 illustrates the hold-current and trip-current behaviour of PTC devices as a function of device bulk temperature.

**Region A** represents the combinations of current and temperature at which the PTC device will trip (go into the high-resistance state) and protect the circuit. **Region B** describes the combinations of current and temperature at which the PTC device will allow for normal operation of the circuit, a low resistance state. In **Region C**, it is possible for the device to either trip or remain in the low-resistance state, depending on the individual device resistance. The boundaries between these regions are defined as

- \( IHOL \) hold current, at a given temperature, is the highest steady-state current that a device will hold for an indefinite time without transitional tripping from the low resistance to the high resistance state.
- \( IT_{MIN} \) is the minimum current at which the device will switch from the low resistance to the high resistance state.

The trip current is typically greater than the normal operating current. Unlike time-to-trip, the hold current of a device is a steady-state condition that can be fairly accurately defined by the heat transfer environment. Under steady-state conditions, equation (10.63) is valid and the \( IR \) heat generated equals the heat lost to the environment. Therefore, if \( U \) increases, the hold current increases, with the approximate dependency:

\[
I_H = \sqrt{U}
\]

### Time-to-trip

The time-to-trip of a PTC device is the time it takes for the voltage drop across the device to rise to greater than 80 percent of the voltage of the power source, or when the resistance of the device increases substantially relative to the load resistance. A trip event is caused when the rate of heat lost to the environment is less than the rate of heat generated, causing the device temperature to increase. The rate of temperature rise and the total energy required to make the device trip, depend on the fault current and the heat transfer environment.

For low-fault currents, for example two-to-three times the hold current, devices trip slowly since a substantial amount of the \( IR \) energy generated is retained in the device, thereby rapidly increasing its temperature. A trip event of this kind can be regarded as an adiabatic trip event. Under these conditions, the heat transfer to the environment is less significant in determining the time-to-trip of the device.

As tripping is a dynamic event, it is difficult to precisely predict the change in the time-to-trip since a change in the heat transfer coefficient is often accompanied by a change in the thermal mass around the device. For example, the device uses a metal heatsink, not only will the heat transfer increase, but the device will also need to heat some fraction of the metal (due to the intimate thermal contact) before the device will trip. Therefore, not only is the thermal conductivity of the metal important, but the heat capacity of the metal is also a factor in determining the time-to-trip.

The switching time or time-to-trip \( t_s \) can be approximated, in an adiabatic condition, by:

\[
t_s = \frac{C}{P} (T_R - T_A)
\]

This equation shows that the switching time is influenced by the size of the PTC thermistor, its reference temperature, and the power supplied. Switching times are lengthened by increasing the voltage or the reference temperature; while a high power consumption by the PTC thermistor results in shorter switching times.

**Figure 10.26**. Polymeric PTC curves for a PTC rated at 72V, 40A, with a 1.1A to 3.75A hold current.
Figure 10.26 shows a typical pair of operating curves for a PTC device in still air at 0°C and 75°C. The curves are separable because the heat required to trip the device comes both from electrical $I^2R$ heating and from the device environment. At 75°C the heat input from the environment is substantially greater than at 0°C, so the additional $I^2R$ needed to trip the device is correspondingly less, resulting in a lower trip current at a given trip time, or a faster trip at a given trip current.

**Device reset time**

In Figure 10.27, after a trip event (when the current fault condition has been alleviated), the resistance recovery to a quasi-stable low value is rapid, with most of the recovery typically occurring within a few minutes. Figure 10.27 shows the resistance recovery curve and associated power dissipation for a family of leaded PTC fuse devices. As with other electrical properties, the resistance recovery time depends upon both device design and the thermal environment. Since resistance recovery is related to device cooling, the greater the heat transfer, the quicker the recovery.

![Resistance recovery curve](image)

**Typical recovery after a trip event:** trip jump, $R_{MAX}$

PTC devices exhibit resistance hysteresis after tripping, either through an electrical trip event or through a thermal event such as reflow soldering. Figure 10.27 shows typical polymeric PTC device behaviour after tripping and when cooling. It can be seen that even after a number of hours, the device resistance is still greater than the initial pre-trip resistance. Over an extended period, device resistance will continue to fall and will eventually approach the initial resistance. Therefore, when PTC devices are being used, this ‘trip jump’ or ‘reflow jump’ is taken into consideration when determining the hold current. This increase in resistance is defined as $R_{MAX}$ and the jump is measured hour one hour after the thermal fault event. The long-term cold resistance of polymeric PTC thermostors increases with successive trip events.

**10.3.2ii Ceramic PTC devices**

Unlike PTC thermostors made of plastic materials, that is, polymeric materials, ceramic PTC thermostors always return to their initial resistance value, even after frequent heating/cooling cycles. The thermal properties and many of the electrical properties are characterised the same for both PTC and ceramic types.

**Ceramic PTC thermostors**

Mixtures of barium carbonate, titanium oxide and other materials (become doped polycrystalline ceramic, containing $\text{BaTiO}_3$ - 69% plus tianlates of $\text{Pb}$ - 15%, $\text{Sr}$ - 10%, $\text{Ca}$ - 5% and 1% dopants), whose composition produces the desired electrical and thermal characteristics are ground, mixed and compressed into various shapes. These blank parts are then sintered, at temperatures just below 1400°C, and after cooling, they are contacted, provided with connection elements, and finally coated or encased. Multilayer or bulk ceramic types are available.

Generally, ceramic is a good insulating material with a high resistance. Semi-conduction and thus a low current flow are achieved by doping the ceramic with materials of a higher valency than that of the crystal lattice. Some of the barium and titanate ions in the crystal lattice are replaced by these higher valencies in order to obtain a specified number of free electrons which make the ceramic conductive.
Switch temperature, $T_s$

The switch temperature of a ceramic PTC is the temperature at which the resistance of the PTC thermistor begins to increase rapidly. The switch temperature is usually defined as the temperature where the resistance of the element is twice the minimum resistance value $R_{min}$. $T_s = (2 \times R_{min})$.

Transitional temperature coefficient, $\alpha$

The transitional temperature coefficient $\alpha$ is defined as the relative change in resistance referred to the change in temperature and is calculated for each point on the resistance versus temperature curve by:

\[ \alpha = \frac{1}{2} \frac{d \ln R}{d T} = \frac{\ln R_2 - \ln R_1}{T_2 - T_1} \approx \frac{\ln R_2 - \ln R_1}{R_2 - R_1} \frac{d R}{dT} \]

Within this temperature range, the inverse relation gives:

\[ R_1 \leq R_{min} < R_2 \rightarrow \alpha = \frac{\ln R_2 - \ln R_1}{R_2 - R_1} \alpha = \frac{\alpha}{R_2 - R_1} \]

The value of $\alpha$ for the individual types relates only to the temperature range in the steep region of the resistance curve, which is the region of primary interest for most applications.

Voltage dependence of resistance

Higher voltage applied to the ceramic PTC thermistor drop primarily at the grain boundaries with the result that the high field strengths dominate in these regions break-down the potential barriers, thus producing a lower resistance. The higher the potential barriers, the greater the influence of this ‘varistor effect’ on resistance. Below the reference temperature, most of the applied voltage is supported across the grain resistance. Thus the field strength at the grain boundaries decreases and the varistor effect is quite weak.

These mechanisms result in the increase of alpha and decreases the pre and post trip resistance as the field strength increases as shown in figure 10.28c.

Frequency dependence of resistance

Due to the structure of the PTC thermistor ceramic material, on ac voltages it is not a pure ohmic resistor. It acts as a capacitive resistor because of the grain boundary junction depletion layers. The impedance measured with ac voltages decreases with increasing frequency, as shown in figure 10.28b. The dc tripped resistance is reduced by a factor of over 50 when the element is used at 1kHz, so use of the PTC is generally restricted to DC and line frequency operation.

Protection circuit operation

Figure 10.29 illustrates the two operating states of a PTC fuse. During rated operation of the load the PTC resistance remains low, operating Point f in figure 10.24. Upon overloading or shorting of the load, however, the power consumption in the PTC thermistor increases so much that it heats up, its resistance increases dramatically, and this reduces the current flow to the load to an admissible low level, operating Point 4 in figure 10.24. Most of the source voltage $V_s$ is then impressed across the PTC thermistor. Although the current is reduced it is sufficient to maintain the PTC in the high-resistance mode, ensuring protection until the cause of the over-current has been removed.

Figure 10.29 illustrates the load-line operating principle of a PTC thermistor designed to operate as a resettable fuse. The region indicated as ‘A’ represents the normal range of current operation. When current exceeds $I_{max}$ the device self-heating increases its resistance and causes the circuit to operate in the region indicated by B.

The position of the circuit load-line can be designed such that the over-current protection is either automatically reset or requires a manual reset. In the automatic reset mode, the load line intercepts the V-I characteristic at the point F. Stable operation can only occur at this point for normal loads.

In the manual reset mode, the load line intercepts the V-I characteristic at three points in figure 10.29: C, D, and E. Point D is unstable so, in practice, stable operation only occurs at points C and E.

PTC device application

Some of the types of applications that utilize the self-heated characteristics of the PTC thermistor include:

- self-regulating heaters
- over-current protection
- liquid level sensing
- constant current
- time delay
- motor starting
- arc suppression

Generally the device cross-sectional area determines the surge current capability, and the device thickness determines the surge voltage capability. Polymer PTC devices typically have a lower resistance than ceramic PTCs which are stable with respect to voltage and temperature. After experiencing a fault condition, a change in initial resistance occurs with the polymeric PTC.
PTCs are automatically resettable whereas traditional fuses need to be replaced after they are tripped, with most similar over-current events are expected to occur often, and where maintaining low warranty and service costs, constant system uptime, and/or user transparency are at a premium. They are also often chosen in circuits that are difficult to access in or remote locations, were fuse replacement or MCB reset would be difficult. There are several other operating characteristics to be considered that distinguish PTCs and fuses, and it is also best to test and verify device performance before use within the end application.

Table 10.2: Characteristics of polymeric and ceramic PTC thermistor fuse devices

<table>
<thead>
<tr>
<th>PTC Thermistor material</th>
<th>nominal Ohms</th>
<th>Maximum voltage current trip</th>
<th>resistance stability (with voltage and temperature)</th>
<th>resistance change after surge</th>
<th>typical application</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polymer PTC Thermistor</td>
<td>0.01 - 20</td>
<td></td>
<td>Good</td>
<td>10 - 20%</td>
<td>Industrial equipment</td>
</tr>
<tr>
<td>Ceramic PTC Thermistor</td>
<td>10 - 50</td>
<td>600V, 13A</td>
<td>R decreases with temperature and under impulse</td>
<td>small</td>
<td>Balanced line</td>
</tr>
</tbody>
</table>

Example 10.9: Resettable ceramic fuse design

A 24V transformer, operating in an ambient temperature range of 20°C to 60°C, is to be PTC thermistor protected under the following conditions:

1. Normal current = 80mA
2. Fault current = 300mA

Determine if a 50V, 20Ω ceramic device with the following characteristics, is suitable.

The trip current, the minimum must-switch current, is given by

$$I_{op} = \frac{\delta \times (107 - 0.85 \times T) \times 0.8 \times R_{PGC}}{0.8 \times 20^\circ C}$$

The hold current, the maximum no-switch current, is given by

$$I_{oh} = \frac{\delta \times (93 - 0.85 \times T) \times 1.2 \times R_{PGC}}{1.2 \times 20^\circ C}$$

where:

- $\delta = 0.008$ is the dissipation factor
- $R_{PGC} = 20\Omega$ is the nominal resistance at 25°C

Solution

For this application, the requirements are, a PTC element rated for at least 24V, 50/60Hz, can carry 80mA in a 60°C ambient, and will switch when conducting less than 300mA at 20°C.

1. The device maximum rated rms voltage must be greater than the application operational voltage:
   - $V_{in} > V_{app, max}$
   - 50V ac > 28V ac

2. The trip current must be less than the fault current, 300mA:
   - $I_{op} < I_{sw}$
   - $I_{op} < 0.008 \times (107 - 0.85 \times T) \times 0.8 \times R_{PGC} / 0.8 \times 20^\circ C$
   - $I_{op} < 0.21A < 0.30A$

3. The hold current (current without switching) must be greater than the normal operating current, 80mA:
   - $I_{oh} > I_{app, max}$
   - $I_{oh} > 0.008 \times (93 - 0.85 \times T) \times 1.2 \times R_{PGC} / 1.2 \times 20^\circ C$
   - $I_{oh} > 0.12A > 0.08A$

The selected PTC fuse is suitable for this transformer protection case.

Traditional Fuses versus PTCs

Fuses and PTC devices are both over-current protection devices, though each offer their own unique operating characteristics and benefits. Understanding the differences between the two technologies makes the selection choice easier, depending on the application. The most obvious difference is that PTCs are automatically resettable whereas traditional fuses need to be replaced after they are tripped, and they will not actually interrupt the current flow when tripped, and this open circuit results in no leakage current when subjected to an overload current. A PTC resettable fuse has better defined characteristics in low voltage ac applications, than traditional fuses, in terms of arcing and resultant circuit voltages with inductive circuits.

3.3.3 Summary of over-current limiting devices

Over-current protection technologies are summarized in Table 10.3, and as follows:

- PTC thermistors provide self-resetting protection.
- Fuses and MCBs provide good overload capability and low resistance.
- Heat coils protect against lower level ‘sneak currents’.
- LFRs provide the most fundamental level of protection, combined with the precision resistance values needed for balanced lines and are often combined with other devices.

The miniature circuit breaker, MCB, a mechanical current controlling device, is considered in 28.19.

Table 10.3: Summary of over-current limiters

<table>
<thead>
<tr>
<th>action</th>
<th>type</th>
<th>performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reducing series</td>
<td>Polymer PTC</td>
<td>reset, fastest, good, poor</td>
</tr>
<tr>
<td></td>
<td>Ceramic PTC</td>
<td>reset, fast, good, low</td>
</tr>
<tr>
<td>interrupting series</td>
<td>Fuse</td>
<td>disconnected, slow, fair, good</td>
</tr>
<tr>
<td></td>
<td>Line feed</td>
<td>both lines disconnected, poor, good</td>
</tr>
<tr>
<td>diverting series/shunt</td>
<td>Heat coil</td>
<td>shorted or open, slow, poor</td>
</tr>
<tr>
<td></td>
<td>Thermal switch</td>
<td>shorted, poor, good, high</td>
</tr>
</tbody>
</table>

Table 10.3: Summary of over-current limiters
10.4 Overvoltage

Voltage transients in electrical circuits result from the sudden release of previously stored energy, such as with insulation breakdown arcing, fuses, contactors, freewheeling diode current snap, switches, and transformer energising and de-energising. These induced transients may be repetitive or random impulses. Repetitive voltage spikes are observable but random transients are elusive, unpredictable in time and location. A spike is usually brief but may result in high instantaneous power dissipation. A voltage spike in excess of a semiconductor rating for just a few microseconds usually results in catastrophic device failure. Extensive noise may be injected into low-level control logic causing spurious faults. Generally, high-frequency noise components can be filtered, but low-frequency noise is difficult to attenuate.

Overvoltage devices are placed in parallel with a load or circuitry to be over-voltage protected, to limit the magnitude of the voltage that can appear across the input to a circuit. The overvoltage device appears as a very high-impedance (virtually an open circuit) under normal operating conditions. When an overvoltage event occurs, however, the overvoltage device changes its impedance to divert current through itself, around the protected circuit.

Overvoltage protection devices are designed to protect circuits and additionally, they must:

- Not interfere with normal circuit operation.
- Provide maintenance-free operation.
- Reduce long-term cost of the installation by minimizing maintenance time and system downtime.
- Allow the designer to meet industry standards.

Effective transient overvoltage protection requires that the impulse energy be dissipated in the parallel added transient absorption circuit at a voltage low enough to afford circuit survival.

Clamping and Crowbar Devices

Over-voltage protection devices can be classified as either clamping or fold-back (or crowbar). Zener diodes and metal oxide varistors are clamping devices, since they attempt to clamp the voltage at a defined voltage during a stress event. A crowbar device, such as gas discharge tubes and thyristor surge suppressors attempt to create a short circuit when a trigger voltage is reached, with both cases illustrated in Figure 10.30.

Crowbar devices with low on-state voltage can keep voltage levels well below the critical values for sensitive electronic elements and carry considerable current without self-damage due to power dissipation. The lowest current and voltage point that can sustain the on-state of the crowbar device is known as the holding point, as seen Figure 10.30. If the electrical node being protected can supply the voltage and current levels of the holding point, a crowbar device may not turn off after the electrical stress has been removed. The crowbar device must ensure the protection turns off when the electrical stress is removed and does not turn on during normal operation.

Voltage clamp devices do not have the problem of not turning off after a stress event. Clamping devices protecting dissipate considerable power, which is dissipated internally. Clamping devices need a low dynamic resistance in the on-state to ensure that while carrying large currents the voltage does not exceed the allowed levels for the sensitive circuit elements.

Two voltage transient suppression techniques can be employed.

- **Transient voltage attenuation**

  Low pass filters, such as an L-C filter, can be used to attenuate high frequencies and allow the low-frequency power to flow.

- **Diverter (to limit the residual voltage)**

  Voltage clamps such as crowbars or snubbers are usually slow to respond. The crowbar is considered in section 10.2.3 while the snubber, which is for low-energy applications, is considered in sections 8.2 and 8.3.

The voltage-limiting function may be performed by a number of non-linear impedance devices such as reverse selenium rectifiers, avalanche (commonly called Zener) diodes, and varistors made of various materials such as silicon carbide or zinc oxide.

The relationship between the current in the non-linear device, \( I \), and the voltage across its terminals, \( V \), is typically described by the power law

\[
I = kV^\alpha
\]

where \( k \) is an element constant dependent on device geometry and material in the case of the varistor, and the non-linear exponent \( \alpha \) is defined as

\[
\alpha = \frac{\log I_2 - \log I_1}{\log V_2 - \log V_1} = \frac{\log I_1/I_2}{\log V_1/V_2} = \frac{1}{\log V_1/V_2} \tag{10.66}
\]

where \( I_1 \) and \( I_2 \) are taken a decade apart, \( I_1/I_2 = 10 \). The term \( \alpha \) represents the degree of non-linearity of the conduction. The higher the value of \( \alpha \), the better the clamp and therefore alpha may be used as a figure of merit. Linear resistance has an alpha of 1 and a conductance of \( \frac{1}{\alpha} \).

The non-linear voltage-dependent static and dynamic resistances are given by

\[
R = \frac{V}{I} = \frac{V}{kV^\alpha} = \frac{1}{\alpha} \cdot V^{\alpha+1} \tag{10.68}
\]

and the power dissipation is

\[
P = V I = V kV^\alpha = k \cdot V^{\alpha+1} \tag{10.70}
\]

The most useful transient suppressors are the Zener diode and the varistor. They are compact devices which offer nanosecond response time and high energy absorption capability.

1 - **The Zener diode**, usually called a transient voltage suppressor, TVS, in voltage suppression applications, is an effective clamp and comes the closest to being a constant voltage clamp, having an
alpha of 35. Since the avalanche junction area is small and not highly uniform, substantial heating occurs in a small volume. The energy dissipation of the Zener diode is limited, although transient absorption Zener devices with peak instantaneous powers of 50 kW are available. These peak power levels are obtained by:

- Using diffusion technology, which leads to low metallisation contact resistance, nature width, and minimises the temperature coefficient.
- Achieving void-free soldering and thermal matching of the chip and the large area electrodes of copper or silver. Molybdenum buffer electrodes are used.
- Using bulk silicon compatible glass passivation which is alkali metal contamination free, and is cut without glass cracking.

Voltage ratings are limited to 280V but devices can be series connected for higher voltage application. This high-voltage clamping function is unipolar and back-to-back series connected Zener diodes can provide high-voltage bipolar symmetrical or asymmetrical voltage clamping.

2. The varistor (variable resistor) - voltage-dependant resistance inversely related to voltage) is a ceramic, bipolar, non-linear semiconductor utilising silicon carbide for continuous transient suppression or sintered zinc oxide for intermittent dissipation. Approximately 90 per cent by weight of zinc oxide and suitable additives such as oxides of bismuth, cobalt, manganese and other metal oxides, when pressed, can give varistors with alphas better than 25. The micro-structure of the plate capacitor like body consists of a matrix of highly conductive (and high thermal conductivity) zinc oxide grains separated by highly resistive inter-granular grain boundaries of the additive oxides. Micro-varistors are only produced where the sintered zinc oxide grains meet, providing pn junction semiconductor-type characteristics, as shown in figure 10.32a. The grain sizes vary from approximately 100µm in diameter for low-voltage varistors down to 10µm for high voltage components, producing 30 to 250V/mm (typically 2V to 3V per grain boundary junction). The junctions block conduction at low voltage and provide non-linear electrical characteristics at high voltage. Effectively pn junctions are distributed in parallel and series throughout the structure volume, giving more uniformly distributed heat dissipation than the plane structure Zener diode. The diameter (parallel conduction paths over the area) determines current capability, hence maximum power dissipation, while thickness (number series connected micro-varistors) specifies voltage, as indicated by the I-V characteristics in figure 10.32b. A greater number of adjacent boundaries in series and parallel (that is, the volume of the device) leads to higher energy absorption capability. The structure gives high terminal capacitance values (which decreases with voltage rating according to $V^{2}$) depending on area, thickness, and material processing. The varistor may therefore be limited in high frequency applications (>1kHz), due to $C V^{2}$ related losses. Functionally the varistor is similar to two identical Zener diodes connected back-to-back, in series.

![Figure 10.32. Varistor: (a) conduction mechanisms and (b) I-V linear characteristics.](image)

Figure 10.33a shows the general equivalent circuit models for the varistor, which consists of the inter-granular boundary resistance $R_{BG}$ ($\rho = 10^{3}$ to $10^{5}$Ωcm) and the ohmic bulk resistance $R_{B}$ of the zinc oxide ($\rho = 1$ to 100Ωcm), and the non-linear varistor resistance $R_{VAR}$ (0 to $\infty$Ω).

Leakage current region, $I < 10^{-4}$

Figure 10.33b shows the model when the inter-granular boundary resistance $R_{BG}$ dominates the resistance $R_{BG} << R_{B}$, giving $\alpha = 1$, as shown in figure 10.34a. $R_{B}$ is temperature (negative) dependent, decreasing with temperature, producing increased leakage current, hence higher steady-state standby losses.

![Figure 10.33b. Varistor equivalent circuit models: (a) complete model; (b) low current; (c) normal operating region model; and (d) high current model.](image)

The inter-granular capacitance $C$, measured at 1kHz and has a positive temperature coefficient, <0.1%/K, increases with increased thickness (increased voltage rating) and decreases with increased area (increased current/power rating). The capacitance acts as a high pass filter, but restricts the operating frequency limit due to $\frac{1}{2}CV^{2}$ transferred losses.

The lead inductance ($\approx 1nH/mm$) $L$ limits the element transient response ($L/R_{VAR}$), hence lead length should be minimised.

The varistor voltage rating is the voltage drop across the element when the current is 1mA, at 25°C.

![Figure 10.34. Varistor: (a) I-V linear and (b) static resistance characteristics.](image)

10.4.1i - Comparison between Zener diodes and varistors (also see Chapter 13.1.3i)

Figure 10.35a illustrates the I-V characteristics of various voltage clamping devices suitable for 240 V ac application. The resistor with alpha equal to 1 is shown for reference. It is seen that the higher the exponent alpha, the nearer an ideal constant voltage characteristic is attained, and that the Zener diode performs best on these grounds. When considering device energy absorption and peak current and voltage clamping level capabilities, the Zener diode loses significant ground to the varistor.
The higher the alpha, the lower will be the standby power dissipated. Figure 10.35b shows the dependence of standby power dissipation variation on withstand voltage for various transient absorbers. A small increase in Zener diode withstand voltage produces a very large increase in standby power dissipation. Various device compromises are borne out by the comparison in Table 10.4. The current, power, and energy ratings of varistors typically are rated values up to 85°C, then linearly derated to zero at a case temperature of 125°C. Voltage-limiting diodes are typically linearly derated from rated values at 75°C to zero at 175°C. Reliability depends on the ambient temperature and applied voltage, and lifetime decreases with increased voltage or temperature. In the case of the varistor, an 8 percent increase in applied voltage halves the mean time between failures, mtbf, for applied voltages less than 0.71 times the nominal voltage. Below 40°C ambient, the mtbf for a varistor is better than 7 x 10^9 hours (0.7 fit).

The voltage temperature coefficient for the varistor is -0.05 per cent/K while +0.1 per cent/K is typical for the power Zener (at 1mA).

The following design points will specify whether a Zener diode or varistor clamp is applicable and the characteristics of the required device.

- Determine the necessary steady-state voltage rating.
- Establish the transient energy to be absorbed by the clamp.

In order to meet higher power ratings, higher voltage levels or intermediate voltage levels, Zener diodes or varistors can be series-connected. The only requirement is that each series device has the same peak current rating. In the case of the varistor this implies the same disc diameter. Then the I-V characteristics, energy rating, and maximum clamping voltages are all determined by summing the respective characteristics and ratings of the individual devices.

Parallel operation is difficult and matched I-V characteristics are necessary. A feature of varistors often overlooked is deterioration, which is not applicable to TVS diodes. Figure 10.36a shows that at relatively low energy levels an infinite number of transients can be absorbed, while at rated absorbed energy only one fault is allowed. This single fault, lifetime, is defined as that energy level that causes a 10 per cent increase in clamping voltage level, for a specified current density.

The failure mode of the Zener diode and varistor is a short circuit. Subsequent high current flow may cause an explosion and disintegration of contacts, forming an open circuit. This catastrophic condition can be avoided by fuse protection. Semiconductor based devices deteriorate minimally.
Selenium suppressors

Selenium, a naturally occurring substance, has been used as a semiconductor in rectifiers and suppressors. Although its popularity as a rectifier has virtually ceased in favour of its silicon equivalent, demand for selenium suppressors continues.

Depositing the elements on a metal substrate’s surface produces selenium cells. This provides the cells with good thermal mass and energy dissipation as well as ‘self-healing’ characteristics, allowing the device to survive energy discharges in excess of the rated value. Selenium’s crystalline structure gives it the ability to continue functioning after a burst of energy in excess of its short pulse width rating. Its suppressor operation is comparable to a pressure relief valve – when the pressure rises, the relief valve opens, releases the pressure, and then resets itself.

Because of its unique properties, the selenium suppressor remains viable in many applications. Its transient voltage clamping characteristic, its ability to continuously dissipate power and handle long surges, makes it better than MOVs or silicon suppressors for some applications.

### Table 10.4: Comparison of typical transient suppressor characteristics

<table>
<thead>
<tr>
<th>Suppressor type</th>
<th>Standby current (mA)</th>
<th>Peak current at 1ms (kA)</th>
<th>Peak energy (W)</th>
<th>Voltage clamping ratio at 10μA (V)</th>
<th>Voltage range (V)</th>
<th>Capacitance at 1MHz (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon carbide varistor</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>15-300</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Selenium</td>
<td>12</td>
<td>30</td>
<td>9</td>
<td>2.3</td>
<td>35-700</td>
<td>-</td>
</tr>
<tr>
<td>Metal oxide varistor</td>
<td>1</td>
<td>120</td>
<td>40</td>
<td>1.7</td>
<td>14-1200</td>
<td>2</td>
</tr>
<tr>
<td>Zener diode (5W)</td>
<td>0.005</td>
<td>5.5</td>
<td>1.5</td>
<td>2.0</td>
<td>1.4</td>
<td>1.8-280</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Suppressor type</th>
<th>Peak current at 1ms (kA)</th>
<th>Peak energy (W)</th>
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<td>-</td>
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<td>-</td>
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<tr>
<td>Selenium</td>
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<td>9</td>
<td>2.3</td>
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<tr>
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<td>5.5</td>
<td>1.5</td>
<td>2.0</td>
<td>1.4</td>
</tr>
</tbody>
</table>

The selenium suppressor can absorb energy levels in excess of its rated capability while maintaining its clamping characteristics subsequent cycles. The layering of the suppressor onto the aluminium plate allows the suppressor’s energy capabilities to follow that of a heat sink thermal curve. This heat sink capability allows steady-state power dissipation up to 40 times that of an MOV. For a 130V suppressor, the selenium suppressor allows steady-state dissipation of 2.5W to 80W, compared with an MOV that allows only 0.1W to 2.5W.

Selenium suppressor cell plates are available in sizes varying from less than 20mm x 20mm to in excess of 30mm x 30mm that can function at a temperature of 0°C to 55°C ambient without any derating. The voltage of a selenium suppressor cell starts at 28Vrms or 22.5Vdc per cell plate, with a 75V maximum due to the dielectric ceiling of the cell. The capacitor plate nature allows placement in series to attain higher voltage levels. Other suppressors can handle high current, short pulse widths in the microsecond range, but the selenium suppressor can handle milli-second pulse width currents, making it a slower but a more robust suppressor than silicon devices. It has a typical response time of less than 1ms and is capable of handling pulses with long decay times as experienced with the switched fields of large DC motors or any inductive loads with L/R ratios in the 100ms range, such as with power conditioning systems (that is, from power strips to a service entrance), generators, AC controllers, on the DC side of a rectified generator output, across SCR's on large controllers, and on transformers for line-to-line transient suppression.

### Fundamentals of overvoltage protection theory

Electronic equipment and components have been designed to function properly when used within their specified current and voltage ratings. When these ratings are exceeded during operation, the equipment or components may sustain permanent damage and may cease to operate. Common sources of overvoltage conditions are lightning, ac power contact, and power induction. Other electrical components may be susceptible to shifts in system ground potential, increasing the need for overvoltage protection. Voltage protection devices may be installed in parallel with the equipment or components to be protected. In the event of an overvoltage condition, protection devices switch rapidly from a high to a low impedance state, thus clamping the transient voltage across the components to a safe operating level. Under normal operating conditions, the overvoltage device appears as a high impedance device (virtually open circuit, with minimal leakage current) and does not affect normal system operation.

#### Example 10.10: Non-linear voltage clamp

Evaluate the current of a 1mA @ 250V Zener diode when used to clamp at 340V dc. At 340V dc, calculate the percentage decrease in voltage-dependent resistance and the per unit increase in power dissipation, assuming α = 30.

**Solution**

i. From \( I = \frac{kV}{V} \) (equation (10.66)),

\[ I_Z = I(V/V) = 1 \text{mA (340V/250V)} = 10.14 \text{A} \]

The Zener diode will conduct 10.14A when clamping at 340V (a 10,140 increase on the standby current of 1mA).

ii. From equation (10.68), \( R = \frac{V}{V} \) therefore

\[ \frac{1}{R} = \frac{1}{V} - \frac{1}{V_{Z}} = \frac{1 - \frac{340V}{250V}}{340V} = 0.99987 \]

The percentage decrease in resistance is 99.987 per cent.

The static resistance decreases from (250V / 1mA) 250kΩ to (340V / 1.14A) 33.5Ω.

By differentiating equation (10.66), the incremental resistance (dv/di) reduces to 1.12Ω (33.5Ω/30).

iii. \( P = kV^{\alpha} \) (equation (10.70)),

\[ P = 340V^{10.14} = 13793.5 \text{W} \]

The per unit power increase is 13,800.

The power increases from (250V x 1mA) 0.2 W at 250V standby to (340V x 10.14A) 3447.6 W when clamping at 340V dc.

#### 10.4.2 Transient voltage fold-back devices

A fold-back device is normally in a high-resistance state for voltages below the break-over voltage. In this state little current flows through the device. When the voltage exceeds the break-over voltage, the device folds back or goes into a low-impedance state, allowing the device to conduct large currents away from sensitive parallel connected electronics. The device will continue to remain in this low impedance state until the current through the device is decreased below its holding current.
Fold-back devices have an advantage over clamping devices because in the fold-back state, a device maintains its voltage, low capacitance, pulsed and ac discharge current handling capability, as specified in figure 10.39.

Unlike the varistor or Zener diode, the voltage collapses to zero when the external surge voltage exceeds the device internal electric field strength, eventually creating a low voltage (10V) sustained ionised arc, which is only extinguished when the external energy is reduced to zero, as resulting from a voltage reversal in an ac circuit.

A number of transitional stages occur during surge voltage suppression, as shown in figure 10.39.

- When inactive, the surge arrester appears as a low capacitance (<1pF) in parallel with a high resistance, typically 1GΩ, where virtually no current flows.
- When the element spark-over voltage is reached, Ve (devices ranging between 70V and 5kV). The voltage rapidly falls to the glow voltage level Vgl, which is between 70 to 200V with a low current of 10mA, gradually increasing to about 1.5A – region G in figure 10.39.
- As the arrester current increases, transition to the arc voltage Va mode occurs, where the voltage falls to 10V to 35V, independent of the subsequent current – region A. The transition time between the glow and arc region is dependent on the available current of the impulse, the distance and shape of the electrodes, the gas composition, gas pressure, and the proprietary emission coatings.
- As the over-voltage decreases, the arrester current decreases to a level where the arc cannot be sustained. The arc ceased suddenly, passing briefly through the glow region, and finally extinguishing at the voltage Ve, termed the extinguishing voltage.

Response behaviour

The rate of rise of terminal voltage affects the electrical performance, as shown in figure 10.40a. At low dv/dt’s (<1V/µs), the dc spark-over voltage Ve,dc of ignition is determined by the electrode spacing, the gas type and pressure, and the degree of pre-ionization of the noble gas.

At high dv/dt’s, the spark-over voltage exceeds the lower steady-state value, Ve,dc. The ignition-aid coating on the inner cylindrical surface reduces the voltage spread of the resultant impulse spark-over voltage Ve, GDTs have no dv/dt sensitively.

The operating mechanisms are such that the surge arrester is not normally suited to dc-circuit operation (or highly inductive ac loads), since to revert to a high impedance mode, the current must drop below the arc discharge mode minimum level of a few 100mA. For this reason, a fail-safe mechanism is incorporated to expedite the resultant high heating losses that occur with continuous arcing. A spring tension-loaded thermal fuse type mechanism is incorporated to short the two electrodes after melting the separating insulating spacer. Figure 10.40b show the typical short-circuit reaction characteristics as a function of the current flowing through the arrester.

Switching spark gaps

The gas discharge principle used in the voltage surge arrester is also applicable to the three-terminal switching spark gap, figure 10.38. The device is deliberately ignited, by the build-up of the terminal voltage, (devices from a few hundred volts, up to 6kV) to produce extremely fast (<50ns) high current (>1kA) switching operations (>2M operations), over a very wide temperature range, virtually without loss when conducting and a high insulating resistance (>100MΩ) when non-conducting.

The Dark Effect

The first surge on the GDT tube results in a higher breakdown than subsequent successive surges. As the GDT is normally housed in a plastic module and deployed in a dark cabinet, the term was called the dark effect. The initial strike ionizes the gas to make it settle into a consistent breakdown voltage specification. The impact has been reduced by the design geometry and emission coating composition
of the gas tube. The first surge impulse is typically 10% higher than the average impulse let-through voltage. Surge at very high impulse current levels do not experience the phenomenon, which indicates the dark effect is dependent on the surge current and source impedance.

The Spark Effect

The spark effect is due to the arc being of a high enough energy density to cause contaminants (impurities) to be released from the internal materials into the GDT gas atmosphere under a single surge. These contaminants in the gas cause the increase of the dc breakdown voltage by more than 10% between the first two surges. Subsequent surges trigger the ‘getter’ effect of the emission coating that will attract the impurities (contaminants) and reduce the breakdown voltage to the original level. Contaminants suspended in the gas change the gas composition and decrease or increase the breakdown voltage according to the Paschen curve of the particular gas mixture.

GDT Life Cycle

The GDT does wear out due to particulates being dislodged from the electrodes during tube arcing. The impact of the arc across the tube is dependent on the energy strike, so the life of the GDT tube is dependent on the applied impulse to it. The surge ionizing effect charges the tube and therefore attracts the particulates to one end of the tube. This has the effect of changing the electrical properties such as the dc breakdown voltage. The end of life shorting the GDT is caused by the rapid breakdown of the emission coating and the electrode material (metal) that further increases internal contaminants. The free materials in the tube attach themselves to the side of the ceramic body between the two electrodes, thereby causing a ‘virtual short’ between the electrodes.

10.4.2ii Thyristor voltage fold-back devices

Thyristor-based devices initially clamp the line voltage, then switch to a low-voltage on-state. After the surge, when the device current drops below its ‘holding current’, the protecting device returns to its original high impedance (off) state.

Figure 10.41 shows the protection action difference between a device that voltage clamps (diode avalanche breakdown action, figure 10.41a), and a device that initially clamps then voltage folds back to a low impedance state (thyristor action, figure 10.41b). The main benefits of thyristor type protection are lower voltage overshoot and an ability to handle moderate currents without device wear-out or a deterioration mechanism. The disadvantages of thyristor protectors are relatively high capacitance, which is a limitation in high-speed digital applications, and low tolerance of excessive current. Thyristor circuit protectors can act either as secondary protection in conjunction with gas discharge tubes, GDTs, or as primary protection for more controlled environments of lower surge magnitudes.

Figure 10.41. Semiconductor I-V characteristics and switching voltage performance: (a) clamping and (b) fold-back devices.

Figure 10.42. Thyristor physical structure, equivalent circuit and I-V curves for thyristors: (a) an SCR; (b) a pair of anti-parallel SCRs, the triac; and (c) the diac.

The protection capability of an SCR is asymmetrical as shown in Figure 10.42a. In the positive direction, turn-on of the thyristor results in a dramatic decrease in resistance while in the negative direction the thyristor provides voltage clamping action, similar to a diode based TVS device. For protection in both voltage polarities, to provide symmetrical crowbar behaviour, it is necessary to use two anti-parallel thyristors. This can be achieved with a pair of discrete SCRs, or with an integrated structure in a single silicon die that has five doped regions, as illustrated in Figure 10.42. The integrated device is usually called a Thyristor Surge Protection Device (TSPD) and its I-V characteristic is shown in Figure 10.43a. The clamping voltage level of fixed voltage thyristors is set during the manufacturing process. Gated thyristors have their protective level set by the voltage applied to the gate terminal.

In response to a transient surge, the thyristor voltage folds back to provide a low-impedance path to ground. The circuit must have enough impedance to limit the fault current below the peak pulse current ($I_{F}$) rating of the thyristor. The over-current protector typically does not operate during a lightning pulse. Two voltage triggered fold-back silicon semiconductor devices are commonly used for circuit protection: the thyristor surge protection device, TSPD, and the SIDAC (silicon thyristor diode, misnomer) device for alternating current. Both are voltage triggered switches but the TSPD is used to reliably protect telecom lines from high current levels and over-voltage occurrences while a SIDAC (more economically robust DIAC) is intended for use as a triggering device.
The **TSPD** is a silicon structure device typically manufactured on an n-type substrate. It is the equivalent of two SCR’s ‘connected’ in anti-parallel, which allows the flow of electric current in both directions. The TSPD is capable of sinking a surge current pulse to ground when transient voltage appears across its two terminals, occurring when the break-over voltage of the device is reached. The device typically operates symmetrically, protecting in the positive and negative direction. The TSPD turns from the off-state to the on-state based on the breakdown and break-over voltage levels that appear between its two terminals, MT1 and MT2. The devices have a current and voltage curve that has a ‘fold-back’ affect, where the break-over is high, while the clamping voltage is low, basically a short, after the device turns-on giving it high surge abilities. Figure 10.43c shows the symbol for both the TSPD and the SIDAC. The TSPD is a crowbar device, meaning it has two states of functionality: open circuit and short circuit. It is transparent during normal circuit operation, in that it is an open circuit across its two terminals. Most TSPDs are symmetrical bidirectional designs but there are also unidirectional devices with a built in diode, or asymmetric bidirectional TSPDs are available with a reduced break-over trigger voltage in one polarity. Typical TSPD surge current capabilities are up to 200A for a 10/1000μs surge voltage. Operating voltages typically cover a broad range, from 12V up through several hundred volts. They have good dv/dt sensitivity but poor di/dt sensitivity. The main features of TSPDs are:

**Advantages:**
- There is no wear–out (aging) mechanism present as with Gas Discharge Tubes and MOVs
- Very fast turn-on switching
- Electrical parameter consistency (V_{BO}, V_{SS}, I_{BO})
- High immunity to dv/dt conditions (>2kV/μs)
- Compared with the MOV, the total energy dissipated is lower, since the crowbar characteristic is not possessed by MOV devices
- Similar current surge capabilities as the GDT
- Short circuit mechanism for protection of the equipment

**Disadvantages:**
- Very high current surge pulse limitation, where more silicon is needed
- Temperature dependency of the electrical parameters
- Surge performance limited at low temperatures (< -20°C)
- Capacitance is dependent on the die size, but lower than TVS

The **SIDAC**

The SIDAC is a multi-layer silicon semiconductor usually manufactured on a p-type substrate. Being a bilateral device, it switches from a blocking state to a conducting state when the applied voltage of either polarity exceeds the break-over voltage. As with other trigger devices, the SIDAC switches through a negative resistance region to the low voltage on-state and will remain on until the main terminal current is interrupted or falls below the holding current. When the SIDAC switches to the on state, the voltage across the device drops to less than 3V, depending on magnitude of the main terminal current flow. The main application for the SIDAC is ignition circuits or inexpensive high voltage power supplies. The difference between a TSPD and a SIDAC is that the SIDAC is intended to be used as a triggering device. The SIDAC is intended to withstand surge current levels which involves high levels of peak power, such as required by telecommunication protection standards. Most of the applications for the SIDACs are related to capacitor discharge circuitry, as part of a RLC circuit; commonly as lamp starters, strobes and flasher, a stove igniter, etc. The key features of the SIDAC are similar to those of the TSPD. When comparing a similar TSPD with a SIDAC device, the surge current abilities of the TSPD are much larger than the SIDAC. Other key parameters that TSPDs advantageously have over SIDACs are lower leakage current (I_{BO}) and dv/dt immunity.

The I-V curve in figure 10.43b shows the electrical characteristics of a SIDAC. Typical devices are rated at 1A, 220V with junction operating temperatures up to 125°C. Commutation times are better than 100μs and the switching resistance R_s in figure 10.43b, is typically 100Ω.

### 10.4.iii Polymeric voltage variable material technologies

Polymer Electrostatic Discharge (ESD) suppressor devices consist of a polymer embedded with conducting particles as shown in Figure 10.44a. At high voltage, arcs between the particles create a low resistance path resulting in a drop in voltage. Additionally, the polymer suppressors can be manufactured with a gap in an electrode that connects two end terminations. The gap causes the two terminations to be electrically discontinuous (current cannot flow). Into the gap, a polymer-based material is back-filled. This voltage variable material (VVM) has similar electrical characteristics to zinc-oxide material. Under normal circuit conditions, the VVM acts like an insulator, but when an ESD transient occurs, the VVM transits to a conductor and shunts the ESD to ground. Polymer devices are bidirectional crowbar devices as shown in Figure 10.44b.

Polymer ESD suppressor devices are specifically for electrostatic discharge protection of sensitive low voltage technology. ESD is the transfer of electrical charge between any two objects. ESD is different from other, common overvoltage events (switching and surge transients) in that the time it takes ESD to transition from zero to maximum current and voltage is very short. The rise time of an ESD event is less than a nanosecond, while the other transients take longer than a microsecond to reach their peaks. Since polymeric suppressors are generally specifically designed only for ESD protection, they are not capable of withstanding the higher energy levels of surge transients. On the other hand, polymeric products have the lowest capacitance, 0.050pF, of the suppressor technologies and are used to protect high-speed communication lines.

Polymer devices have high bipolar turn-on voltages, usually over 100V, but turn-on quickly, limiting the exposure to high voltage. The working voltage ranges up to 24V dc, with a leakage current of less than 1nA. The operating temperature range is typically from -65°C to +125°C.

### Differences between the GDT and the solid-state semiconductor TSPD thyristor

Static spark-over voltage V_{SO} versus repetitive peak off-state voltage, V_{SM}

Both define the maximum working voltage across the protector before conduction occurs where the protector will have high impedance so that it will not interfere with the normal operation of the system. The DC surge voltage V_{SM} is specified as a typical voltage where the tolerance has to be used to define the minimum rating to not interfere with system’s operating voltage. The TSPD thyristor V_{SM} is specified as an absolute maximum in its data sheets. The DC surge voltage V_{SM} is measured by...
using a slow ramp voltage such as a 100 V/s to 2000 V/s. The $V_{DSS}$ for the TSPD thyristor is measured at a specified current value and is specified as a maximum of 5 μA at the $V_{DSS}$ value.

**Impulse spark-over voltage versus dynamic breakover voltage, $V_{BO}$**

Both define the maximum dynamic protection voltage window of the protectors. The protection voltage is the maximum voltage the system will see. The GDT impulse voltage and the $V_{BO}$ impulse breakover voltage of a TSPD thyristor are specified at a ramp voltage of 100 V/μs or 1000 V/μs. The TSPD thyristor has a tighter maximum working voltage to protection voltage ($V_{DSS}/V_{BO}$) window.

**Impulse discharge current versus non-repetitive peak impulse current**

These two parameters highlight the surge withstand rating of the protector where both are specified using industry standard surge waveforms. The GDT will specify a short circuit current level and the minimum number of operations it can withstand. Although the GDT has much higher impulse surge ratings, the TSPD thyristor does not have a wear-out mechanism like the GDT, so its impulse current ratings are specified as an absolute maximum.

**Capacitance**

Capacitance of a GDT (typically 2pF) is significantly lower than a TSPD thyristor (hundreds of pF). The capacitance of a GDT is not affected by any bias or signal voltages across it and does not change with temperature. A TSPD thyristor or any semiconductor overvoltage protector will have a capacitance dependent on the surge rating (which is dependent on silicon size) and will change according to the bias voltage across it. Thyristor capacitance will also vary with the protection voltage of the same surge rating series, where low $V_{DSS}$ voltage options will have a higher capacitance value.

10.4.3 Protection coordination

Some primary protective devices such as semiconductor-based devices are fast enough to react in time; however these devices tend to have limited current handling capability. Also, semiconductor devices rated for the primary protection task tend to capacitively load a circuit (due to their physically large size) resulting in bandwidth limitations. Non-semiconductor surge protectors, such as the Gas Discharge Tube (GDT), do not capacitively load circuits and can handle very large currents (tens of kA); however, these devices are slower to react and may not keep the voltages sufficiently low to provide successful protection by themselves. Therefore, conventional protection must be based on a number of stages of such devices. These stages typically start with a GDT as the primary protector for its current handling capability, followed by a semiconductor thyristor protector for speed – the secondary protector. When GDT and Thyristor shunt protectors are used as primary and secondary protectors, the protection coordination between them is complicated in practice. When a surge event occurs, the fast secondary protector will act to limit voltage within the system first (due to its speed). Often this protector will be rated to keep the circuit voltages quite low in order to protect the equipment. Thus, its action can prevent the high energy primary protector (GDT), which requires a higher voltage to operate, from working. In this circumstance, damage is likely to occur to the secondary protector before the GDT operates. This problem is solved by the complex process of inter-stage coordination. Coordination is the process of placing impedance between the primary and secondary protectors to ensure that sufficient voltage is generated across the primary protector, resulting from current flowing in the secondary protector, to trigger the primary device. Coordination is engineered properly when the primary protector operates after the secondary protector operates, yet before the secondary protector is damaged. The coordinating impedance can be resistive, capacitive, inductive, non-linear or a combination of all of these; proper selection is critical.

Large resistance is the easiest choice to ensure that only a small current in the secondary device causes a significant voltage across the primary device causing it to operate. However, large resistance introduces considerable loss within the transmission path which is often unacceptable. Capacitance and inductance are also useful, but these impedances are frequency related and so circuits coordinated with such will function only for a band of surge frequencies. Non-linear resistance can also be used to create different coordinating arrangements based on the duration of the surge - low level surges for example which last a long time causing the coordinating impedance to change to a high resistance state choking further current flow and triggering the primary protector (the basis of operation of the PTC).

10.4.4 Summary of voltage protection devices

There is a variety of devices available to provide shunt electrical over-voltage protection to electronic systems and components. Each device has its own characteristics as outlined in figure 10.46 and Table 10.5.
Table 10.5: Features of various protection device technologies. All reset to normal after operation

<table>
<thead>
<tr>
<th>Type</th>
<th>Protection Mechanism</th>
<th>Polarity</th>
<th>Clamp or Crowbar</th>
<th>Speed</th>
<th>Voltage Accuracy</th>
<th>Current Capability</th>
<th>Size / Capacitance</th>
<th>Lowest Trigger Voltage</th>
<th>Isolation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas Discharge Tube</td>
<td>Breakdown of a gas at high voltage</td>
<td>Bidirectional</td>
<td>Crowbar</td>
<td>Slow</td>
<td>Fair</td>
<td>Very high</td>
<td>Large / low</td>
<td>75V</td>
<td>No</td>
</tr>
<tr>
<td>GDT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transient Voltage Suppressor</td>
<td>Non-linear resistance of ceramic or zinc oxide grains</td>
<td>Bidirectional</td>
<td></td>
<td>Fast</td>
<td>Good</td>
<td>Medium to high</td>
<td>Small / medium</td>
<td>80V</td>
<td>No</td>
</tr>
<tr>
<td>MOV</td>
<td>Forward bias and reverse bias diode conduction</td>
<td>Bidirectional</td>
<td></td>
<td>Fast</td>
<td>Poor</td>
<td>Medium to High</td>
<td>Small / medium</td>
<td>NA</td>
<td>Yes</td>
</tr>
<tr>
<td>Polyfiller ESD Device</td>
<td>Wiring between particles in polymer</td>
<td>Bidirectional</td>
<td>Crowbar</td>
<td>Fast</td>
<td>Poor</td>
<td>Low</td>
<td>Small / low</td>
<td>~100V</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Very Fast Surge Events – ESD

10.5 Interference

Electromagnetic phenomenon, whether intentional or unintentional by-products, tend to result in undesirable consequences in power electronic circuits and equipment, in terms of generated noise and susceptibility.

- **EMC - Electromagnetic Compatibility**: The ability of a component or its associated system to operate and function correctly in its intended electromagnetic environment.

- **EMI - Electromagnetic Interference**: Electromagnetic emissions from a component or its associated system that interfere with the normal operation of another component or system, or the emitting component or system itself.

10.5.1 Noise

RFI noise (electromagnetic interference, EMI) and the resultant equipment interaction is an area of power electronic design that is often fraught, under-estimated or overlooked. EMI is due to the effects of undesired energy transfer caused by radiated electromagnetic fields or conducted voltages and currents. The interference is produced by a source emitter and is detected by a susceptible victim via a coupling path. The source itself may be a self-inflicted victim. The effects of this interference can vary from simple intermittent reset conditions to a catastrophic failure.

The coupling path may involve one or more of the following four coupling mechanisms.

- **Conduction - electric current, I**
- **Radiation - electromagnetic field, E**
- **Capacitive coupling - electric field, E**
- **Inductive coupling - magnetic field, H**

10.5.1i - Conducted noise is coupled between components through interconnecting wiring such as through power supply (both ac and dc supplies) and ground wiring and planes. This common impedance coupling is caused when currents from two or more circuits flow through the same wiring. Coupling can also result because of common mode and differential (symmetrical) currents, which are illustrated in figure 10.47. Two forms of common mode currents exist. When the conducting currents are equal such that \( V_{cm1} = V_{cm2} \), then the common mode currents are termed symmetrical, while if \( V_{cm1} \neq V_{cm2} \), then the currents are termed non-symmetrical.

10.5.1ii - Radiated electromagnetic field coupling can be considered as two cases, namely

- **near field**, \( r < \lambda / 2 \pi \), where radiation due to electric fields, \( E \), and magnetic fields, \( H \), are considered separate
- **far field**, \( r \gg \lambda / 2 \pi \), where the coupling is treated as a plane wave.

The boundary between the near and far field is given by \( r = \lambda / 2 \pi \), where \( \lambda \) is the noise wavelength and \( r \) is distance from the source. As a reference impedance, the characteristic impedance of free space in the far field \( Z_0 \) is given by \( E / H \), which is constant, \( \sqrt{\mu / \varepsilon} = 377 \Omega \).

\[
\begin{align*}
\text{(a)} & \quad \text{source} \quad \text{Y}_a \\
\text{(b)} & \quad \text{source} \quad \text{victim} \\
\text{(c)} & \quad \text{Equipment} \\
\text{(d)} & \quad \text{Mains} \\
\end{align*}
\]

Figure 10.47. Common mode & differential mode mains supply noise filtering: (a) differential mode noise paths; (b) common mode noise paths; (c) simple L-C mains filter; and (d) high specification mains filter.

In the **near field** region, the \( r^2 \) (as opposed to \( r^3 \) and \( r^4 \)) term dominates field strength.

- A wire carrying current produces \( E \propto r^2 \) and \( H \propto r^2 \).
- A wave loop carrying current produces \( H \propto r^2 \) and \( E \propto r^2 \).
- The magnetic field \( H \) dominates and the wave impedance \( Z < Z_0 \).

In the near field, interference is dominated by the effective input impedance, \( Z_s \), of the susceptible equipment and the source impedance \( R_s \) of its input drive.

- Electric coupling increases with increased input impedance, while
- Magnetic coupling decreases with increased input impedance.

That is, electric fields, \( E \), are a problem with high input impedance, because the induced current results in a high voltage similar to that given by equation (10.72).

\[
V = I_w R_s \left| Z_s \right| \frac{dV_{cm1}}{dt} \left(10.72\right)
\]
while magnetic fields, $H$, are a problem with low input impedance, because the induced voltage results in a high current similar to that given by equation (10.73)

$$i = \frac{v_i}{R_i} = \frac{\mu_{\text{in}}}{R_i} \frac{dv_i}{dt}$$  \hspace{1cm} (10.73)

In the far field the $r^{-1}$ term dominates. In the far field both the $E$ and $H$ fields are in phase and at right angles. Importantly their magnitudes both decrease, inversely proportionally with distance $r$, so their magnitude ratio remains constant. That is, in the far field the characteristic impedance $Z_0 = E/H = \sqrt{\mu_{\text{in}}/\varepsilon_{\text{in}}} = 120\pi = 377\Omega$ is constant. The far field radiation wave with this constant impedance is termed a plane wave. The electric field component of the plane wave tends to dominate interference problems in the far field region.

### 10.6.1 iii - Electric field coupling

is caused by changing voltage differences, $dv/dt$, between conductors. This coupling is usually modelled by capacitance. The changing electric field produces a current according to $i = C_v dv/dt$, where coupling capacitance $C_v$ is dependant on distance of separation, area, and the permittivity of the media. The mutual inductance $M$ is related to loop area, orientation, separation distance, and screening and its permeability. This induced voltage is independent of any ground connection or electrical connection between the coupled circuits. Magnetic field problems tend to be at low frequencies. Below 100kHz effective screen materials (due to the skin effect) are steel, mu-metal ($\mu_r = 20,000$), and permalloy, while at higher frequencies the good electrical conduction properties of copper and aluminium are more effective despite there much lower permeabilities. For power electronics, circuit noise suppression and interaction is ultimately based on a try-it and see approach. Logic and experience do not necessarily prevail. The noise reduction precautions to follow are oriented towards power electronics applications. Good circuit layout and construction (incorporated at the initial design stage) can greatly reduce the radiated noise, both transmitted and received. Observing starting points are minimising wire loop lengths, using ground planes, capacitor decoupling, twisted wire pairs, and judicious placement of magnetic components. Use opto-couplers, not only to isolate signals but to allow flexible signal grounding that can bypass ground power noise around sensitive circuitry. Sensitive electronic circuitry should be radiation protected by copper (electric) and high frequency magnetic) or mild steel (low frequency magnetic) sheeting, depending on the type of radiation and frequency. Shielding, including electrically isolated heatsinks, should be electrically connected to a point that minimises interference. This may involve connection to supply rails (one of positive, zero, negative) or ground. An R-C snubber across a diode decreases $dv/dt$ while a series inductive snubber will limit $di/dt$. Mains ac supply series input inductors for bridge rectifiers (plus diode R-C snubbers) decrease the amount of diode recovery noise injected back into the mains and into the equipment. Most effective are common mode transformers in all input and output connection cabling. Although differential mode line inductors may be effective in decoupling input power lines, stability issues can arise when used in output cables. Figure 10.48 outlines the frequency bands where the various interference modes can be expected, and the techniques commonly used to suppression that interference.
10.3. Derive the power loss expression for an SCR string with voltage-sharing resistance and an ac supply.

\[ P_L = \frac{V_s^2}{2R} \]

where \( P_L \) is the power loss, \( V_s \) is the supply voltage, and \( R \) is the resistance.

10.4. Two diodes modelled as in figure 2.4a having characteristics approximated in the forward direction by:

\[ V_F = I_F R_F \]

where \( V_F \) is the forward voltage, \( I_F \) is the forward current, and \( R_F \) is the forward resistance.

10.5. In problem 10.4, what single value of resistance in series with each parallel connected diode matches the currents to within 1 per cent of equal sharing? Calculate the resistor maximum power loss.

10.6. A Zener diode has an I-V characteristic described by \( I = kV^n \). What percentage increase in voltage will increase the power dissipation by a factor of 1000? [25 per cent]

10.7. What is the percentage decrease in the dynamic resistance of the Zener diode in question 10.6? [99.845 per cent]

10.8. A string of three 2,600 V thyristors connected in series is designed to withstand an off-state voltage of 7.2 kV. If the compensating circuit consists of a series 33 mF, 0.01 \( \mu \)F snubber in parallel with a 24 kΩ resistor, across each thyristor, and the leakage currents for the thyristors are 20 mA, 25 mA, and 15 mA, at 125°C, calculate the voltage across each thyristor, then the discharge current of each capacitor at turn-on.

10.9. The reverse leakage current characteristics of two series connected diodes are:

\[ I_R = kV^n \]

where \( I_R \) is the reverse current, \( V \) is the reverse voltage, and \( k \) and \( n \) are constants. What is the leakage current in each diode and what resistance is required across diode D2?

10.10. Two high voltage diodes are connected in series as shown in figure 10.5a. The dc input voltage is 5 kV and 10 kΩ dc sharing resistors are used. If the reverse leakage current of each diode is 25 mA and 75 mA respectively, calculate the voltage across each diode and the resistor power loss.

10.11. The forward characteristics of two parallel connected diodes are:

\[ I_F = k(V - V_C) \]

where \( I_F \) is the forward current, \( V \) is the voltage, \( V_C \) is the drop across each diode, and \( k \) is a constant. If the forward voltage of the parallel combination is 1.5V, determine the forward current through each diode.

10.12. Two diodes are connected in parallel and with current sharing resistances as shown in figure 10.7. The forward I-V characteristics are as given in problem 10.11. The voltage across the parallel combination is 2V and the balancing resistors are equal in value. Calculate each diode voltage and current. Calculate resistor maximum power loss. Let \( I_{Rm} = 400A \).