5

Cooling of Power Switching Semiconductor Devices

Semiconductor power losses are dissipated in the form of heat, which must be transferred away from the switching junction. The reliability and life expectancy of any power semiconductor are directly related to the maximum device junction temperature experienced. It is therefore essential that the thermal design determines accurately the maximum junction temperature from the device power dissipation.
Heat can be transferred by any of, or a combination of, three mechanisms, viz., convection, conduction, and radiation.
Electromagnetic thermal *radiation* is given by

$$P_d = \sigma \varepsilon A (T_1^4 - T_2^4) \qquad (5.1)$$

where σ is the Stefen-Boltzmann constant (5.67×10^{-8} W/m^{2}K^4)
ε is a surface property, termed emissivity, see table 5.4
A is the area involved in the heat transfer
T is absolute temperature

The one dimensional model for general molecular heat transfer is given by

$$P_d = -\lambda A \frac{\delta T}{\delta \ell} + \gamma A \ell \frac{\delta T}{\delta t} \qquad \text{(W)} \qquad (5.2)$$

where P_d is the rate of heat transfer (that is, the power dissipated)
$\delta T = T_2 - T_1$ or ΔT, is the temperature difference between regions of heat transfer
λ is thermal conductivity, see Table 5.2
γ is density of the heatsink material
c is specific heat capacity, $\Delta T = W/mc$
ℓ is distance (thickness).

Assuming steady-state heat dissipation conditions, then $\delta T / \delta t = 0$ in equation (5.2).

Conduction through a solid is given by

$$P_d = \frac{\lambda A}{\ell} \Delta T \qquad \text{(W)} \qquad (5.3)$$

Convection heat transfer through fluid or air, under steady-state conditions, is given by

$$P_d = h A \Delta T \qquad \text{(W)} \qquad (5.4)$$

The heat transfer coefficient h ($=\lambda / \ell$) depends on the heat transfer mechanism used and various factors involved in that particular mechanism.
For natural vertical convection in free air the losses for a plane surface may be approximated by the following empirical formula

$$P_d = 1.35 A \sqrt[4]{\frac{\Delta T^5}{\ell}} \qquad \text{(W)} \qquad (5.5)$$

where ℓ is the vertical height in the direction of the air flow.
Two case occur for forced air flow, and the empirical losses are
for laminar flow

$$P_d = 3.9 A \Delta T \sqrt{\frac{v}{\ell}} \qquad \text{(W)} \qquad (5.6)$$

for turbulent flow

$$P_d = 6.0 A \Delta T \sqrt[3]{\frac{v^4}{\ell}} \qquad \text{(W)} \qquad (5.7)$$

where v is the velocity of the vertical air flow.
It is generally more convenient to work in terms of thermal resistance which is defined as the ratio of temperature to power. From equation (5.4), thermal resistance R_θ is

$$R_\theta = \frac{\Delta T}{P_d} = \frac{1}{hA} = \frac{\ell}{\lambda A} \qquad \text{(K/W)} \qquad (5.8)$$

The average power dissipation P_d and maximum junction temperature $T_{j\max}$, plus the ambient temperature T_a, determine the necessary heat sink, according to equation (5.8)

$$P_d = \frac{T_{j\max} - T_a}{R_{\theta j\text{-a}}} \qquad \text{(W)} \qquad (5.9)$$

where $R_{\theta j\text{-a}}$ is the total thermal resistance from the junction to the ambient air. The device user is restricted by the thermal properties from the junction to the case for a particular package, material, and header mount according to

$$P_d = \frac{T_{j\max} - T_c}{R_{\theta j\text{-c}}} \qquad \text{(W)} \qquad (5.10)$$

where T_c is the case temperature, K and
$R_{\theta j\text{-c}}$ is the package junction-to-case thermal resistance, K/W.

An analogy between the thermal equations and Ohm's law is often made to form models of heat flow. The temperature difference ΔT could be thought of as a voltage

drop ΔV, thermal resistance R_θ corresponds to electrical resistance R, and power dissipation P_d is analogous to electrical current I. *[viz., $\Delta T = P_d R_\theta \equiv \Delta V = IR$]*

5.1 Thermal resistances

A general thermal radiation model, or thermal equivalent circuit for a mounted semiconductor is shown in figure 5.1. The total thermal resistance from the virtual junction to the open air, $R_{\theta j\text{-}a}$, is

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + \frac{R_{\theta c\text{-}a}(R_{\theta c\text{-}s} + R_{\theta c\text{-}a})}{R_{\theta c\text{-}a} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a}} \quad \text{(K/W)} \qquad (5.11)$$

In applications where the average power dissipation is of the order of a watt or so, power semiconductors can be mounted with little or no heat sinking, whence

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + R_{\theta c\text{-}a} \quad \text{(K/W)} \qquad (5.12)$$

Generally, when employing heat sinking $R_{\theta c\text{-}a}$ is large compared with the other model components and equation (5.11) can be simplified to

$$R_{\theta j\text{-}a} = R_{\theta j\text{-}c} + R_{\theta c\text{-}s} + R_{\theta s\text{-}a} \quad \text{(K/W)} \qquad (5.13)$$

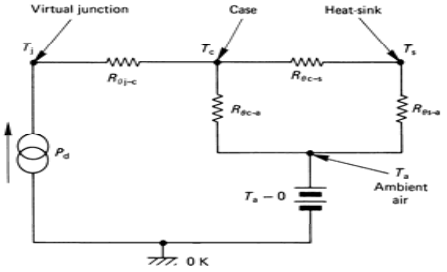


Figure 5.1. *Semiconductor thermal radiation equivalent circuit.*

5.1.1 Contact thermal resistance, $R_{\theta c\text{-}s}$

The case-to-heat-sink thermal resistance $R_{\theta c\text{-}s}$ depends on the package type, interface flatness, mounting pressure, and whether thermal-conducting grease and/or an insulating material is used. In general, increased mounting pressure decreases the interface thermal resistance, and no insulation with thermal grease results in minimum

$R_{\theta c\text{-}s}$. Common electrical insulators are mica, aluminium oxide, and beryllium oxide in descending order of thermal resistance, for a given thickness and area. Table 5.1 shows typical contact thermal resistance values for smaller power device packages, with various insulating and silicone grease conditions.

5.1.2 Heat-sink thermal resistance, $R_{\theta s\text{-}a}$

The thermal resistance for a flat square plate heat sink may be approximated by

$$R_{\theta s\text{-}a} = \frac{3.3}{\sqrt{\lambda \ell}} C_f^{1/4} + \frac{650}{A} C_f \quad \text{(K/W)} \qquad (5.14)$$

Typical values of heatsink thermal conductance λ in W/K cm at 350 K, are shown in Table 5.2 and

ℓ is the thickness of the heat sink in mm
A is the area of the heat sink in cm^2
C_f is a correction factor for the position and surface emissivity of the heat-sink orientation according to Table 5.3.

Table 5.1. Typical case-to-heat-sink thermal resistance value for various packages

Package	*Insulating washer*	$R_{\theta c\text{-}s}$ *(K/W)*	
		Silicone grease	
		with	*without*
TO-3	No insulating washer	0.10	0.3
	Teflon	0.7-0.8	1.25-1.45
	Mica (50 -100 µm)	0.5-0.7	1.2-1.5
TO-66	No insulating washer	0.15-0.2	0.4-0.5
	Mica (50 -100 µm)	0.6-0.8	1.5-2.0
	Mylar (50 -100 µm)	0.6-0.8	1.2-1.4
TO-220	No insulating washer	0.3-0.5	1.5-2.0
	Mica (50 -100 µm)	2.0-2.5	4.0-6.0
TO-247	No insulating washer	0.1-0.2	0.4-1.0
	Mica (50 -100 µm)	0.5-0.7	1.2-1.5

Table 5.2. Thermal conductivity

Material	*λ (W/K cm)*
diamond	2
aluminium	2.08
copper	3.85
brass	1.1
steel	0.46
mica	0.006
beryllium	2.10
oxide ceramic	1.4
$A1_20_3$	0.27
solder (non-lead)	0.44
silicon grease	0.01
still air	0.0004

Table 5.3. Heatsink correction factor

Surface position		
C_f	*Shiny*	*Blackened*
vertical	0.85	0.43
horizontal	1.0	0.50

Table 5.4. Emissivity values

Material	*ε*
Matt surface	0.95
Polished aluminium	0.04
$A1_20_3$	0.15

The correction factor C_f illustrates the fact that black surfaces are better heat radiators and that warm air rises, creating a 'chimney' effect. Equation (5.14) is valid for one power-dissipating device, in the centre of the sink, at a static ambient temperature up to about 45°C, without other radiators in the near vicinity.

In order to decrease thermal resistance, inferred by equation (5.8), finned-type heat sinks are employed which increase sink surface area. Figure 5.2 illustrates graphs of thermal performance against length for a typical aluminium finned heat sink. This figure shows that $R_{\theta s\text{-}a}$ decreases with increased sink length. Minimal reduction results from excessively increasing length as shown in figure 5.2b.

Unless otherwise stated, the heat sink is assumed black and vertically mounted with negligible thermal resistance from case to sink. In accordance with the data in table 5.3, a general derating of 10 to 15 per cent for a bright surface and 15 to 20 per cent in the case of a horizontal mounting position, is usually adopted.

The effective sink thermal resistance can be significantly reduced by *forced air cooling*, as indicated in figure 5.4a and equations (5.6) and (5.7). If the air flow is

- laminar, heat loss is proportional to the square root of air velocity;
- turbulent, velocity to the power of 0.8.

Liquid cooling as shown in figure 5.4b can further reduce effective thermal resistance to as low as 0.1K/W and may provide a much more compact heat-sink arrangement. Both oil and water are used as the coolant and the heat-sink arrangement can either be immersed in the fluid, or the fluid is pumped through the heat sink. The heat can then be dissipated remotely. Water has the advantage of low viscosity, so can be pumped faster than oil. While oil may be inflammable, water corrodes thus requiring the use of de-ionised water with an oxide inhibitor, like antifreeze. Oil emersion has the added advantage of offering possibilities of increasing the breakdown and corona voltage levels, particularly with devices rated above a few kilovolts.

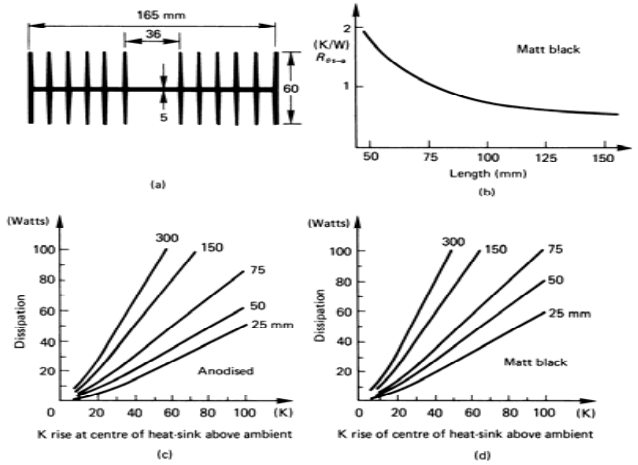


Figure *5.2. Heat-sink typical data:*
(a) cross-section view; (b) heat-sink length versus thermal resistance for a matt black surface finish; (c) temperature rise versus dissipation for an anodised finish and different lengths; and (d) as for (c) but with a matt black surface finish.

Heat pipes are efficient, passive, thermal devices for extracting and remotely dissipating heat. A heat pipe, shown in figure 5.3, is a hollow metal or ceramic tube (for high voltage isolation), typically less than 1mm diameter and a few hundred cm long, closed at each end and containing a dielectric, non-electrical conducting transfer fluid (refrigerant such as methanol, water or Freon when insulation is required) under reduced pressure so as to reduce the fluid boiling point. The component to be cooled is mounted on the evaporator end (the hot end), where the heat boils and expands the liquid to the vapour phase. This vapour rises through the adiabatic tube section to the remote condenser end of the tube (the cold end), taking the heat within it. The vapour condenses back to the liquid phase, releasing its latent heat of vaporisation, and creating a pressure gradient which helps draw more vapour towards the condenser. The temperature difference between the ends may only be a couple of degrees. The remotely situated condenser end is connected to an external heatsink or a radiator type grill, for cooling. The condensed working fluid runs back to the evaporator end due to gravity, or along a wick due to capillary pressure action, depending on the physical

application orientation design for the heat pump. The typical temperature operating range is -55°C to over 200°C.

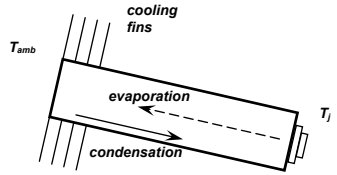


Figure 5.3. *The heat pipe principle.*

The heat power transfer capabilities of a heat pipe are related to its cross-sectional area A and length ℓ according to

$$P = k\frac{A}{\ell} \quad \text{(W)} \tag{5.15}$$

while the temperature difference ΔT between the hot and cold ends is

$$\Delta T = k'P\left(\frac{1}{A_e}+\frac{1}{A_c}\right) \quad \text{(K)} \tag{5.16}$$

where A_e and A_c are the effective evaporator and condenser areas.

5.2 Modes of power dissipation

For long, >1ms, high duty cycle pulses the peak junction temperature is nearly equal to the average junction temperature. Fortunately, in many applications a calculation of the average junction temperature is sufficient and the concept of *thermal resistance* is valid.

Other applications, notably switches driving highly reactive loads, may create severe current-crowding conditions which render the traditional concepts of thermal design invalid. In these cases, transistor safe operating area or thyristor *di/dt* limits must be observed, as applicable.

In yet other applications, intermittent operation in extreme temperature conditions may cause thermal shock and can introduce deep thermal cycling problems with wafer mountings in multi-chip large area packages. Large rapid temperature changes in excess of 80°C, stress the hard solder bonding, causing fatigue and eventual failure after a finite number of cycles N, approximated by

$$N = \frac{k}{A \times \Delta T^2} \tag{5.17}$$

where A is the die area and ΔT is the thermal shock temperature change. The constant k depends on the package, type of hard soldering, etc. Large, multiple die IGBT packages suffer from thermal shock limitations, relatively low reliability, because of the sheer large number of die interconnected over a large area in the module.

Floating silicon wafers in disc type packages suffer from differential thermal expansion.

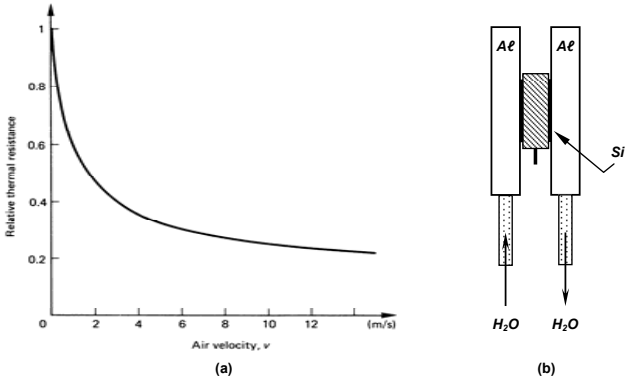


Figure 5.4. *Improved cooling with (a) forced air cooled heat-sink - relative thermal resistance improvement with surface air flow and (b) compact indirect water cooling.*

In a related thermal application, where the power dissipated in the semiconductor consists of pulses at a low duty cycle, the instantaneous or peak junction temperature, not average temperature, may be the limiting condition. Figure 5.5 shows by comparison such a condition, where the operating frequency, not the maximum power dissipated, is dominant in determining junction temperature. In this case *thermal impedance* $Z_{\theta j\text{-}c}$ is used instead of thermal resistance $R_{\theta j\text{-}c}$ such that $Z_{\theta j\text{-}c} = r(t_p)\ R_{\theta j\text{-}c}$, where $r(t_p)$ is the normalising factor yielded from the normalised transient thermal impedance curves for the particular device. Appropriate values for the pulse width t_p and duty cycle factor δ must be used.

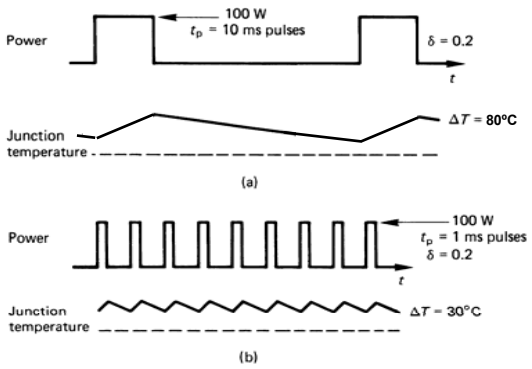


Figure 5.5. Waveforms illustrating that peak junction temperature is a function of switching frequency: (a) lower switching frequency with 10 ms pulse and a 20 per cent duty cycle and (b) high frequency and 1 ms pulse with a duty cycle the same as in (a).

5.2.1 Pulse response

The concept of thermal impedance is based on rectangular power pulses. Non-rectangular pulses are converted to equivalent energy, rectangular pulses having the same peak power, P_p, of period t_p, as shown in figure 5.6. The resultant rectangular power pulse will raise the junction temperature higher than any other wave shape with the same peak and average values, since it concentrates its heating effects into a shorter period of time, thus minimising cooling during the pulse. Worse case semiconductor thermal conditions result.

Figure 5.7 shows the thermal impedance curves for a power switching device, normalised with respect to the steady-state thermal resistance $R_{\theta j\text{-c}}$. The curve labelled 'single pulse' shows the rise of junction temperature per watt of power dissipated as a function of pulse duration. The thermal impedance for repetitive pulses Z, of duty cycle δ, can be determined from the single pulse value z according to

$$Z\left(t_p,\delta\right)=\delta+\left(1-\delta\right)z\left(t_p\right) \qquad \text{(K/W)} \qquad (5.18)$$

The equation (5.10) becomes

$$P_p=\frac{T_{j\max}-T_c}{Z(t_p,\delta)} \quad =\frac{T_{j\max}-T_c}{r(t_p)R_{\theta j-c}} \qquad \text{(W)} \qquad (5.19)$$

Note that the peak power value P_p is employed, and then only for thermal analysis from the junction to the case. That is, $Z_{\theta j\text{-c}}$ is the only thermal impedance that exists.

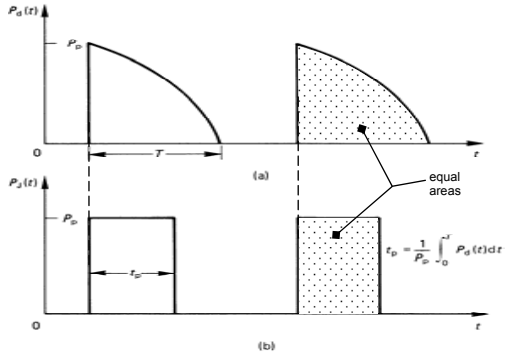


Figure 5.6. *Conversion of non-rectangular power pulse (a) into equivalent rectangular pulse (b).*

5.2.2 Steady-state response

Large cycle-by-cycle temperature fluctuations occur at low frequencies. As frequency increases, thermal inertia of the junction smoothes out instantaneous temperature fluctuations, as shown in figure 5.5b, and the junction responds more to average, rather than peak power dissipation. At frequencies above a kilohertz and duty cycles above 20 per cent, cycle-by-cycle temperature fluctuations usually become small, and the peak junction temperature rise approaches the average power dissipation multiplied by the steady-state junction-to-case thermal resistance, within a few per cent.

Because of thermal inertia, the heat sink responds only to average power dissipation, except at low frequencies. The steady-state thermal conditions for the heat sink are given by

$$P_d=\frac{T_c-T_a}{R_{\theta c\text{-s}}+R_{\theta s\text{-a}}} \qquad \text{(W)} \qquad (5.20)$$

where P_d is the average power dissipation, which is the peak power multiplied by the on-time duty cycle δ for rectangular power pulses. The difficulty in applying equation (5.20) often lies in determining the average power dissipation.

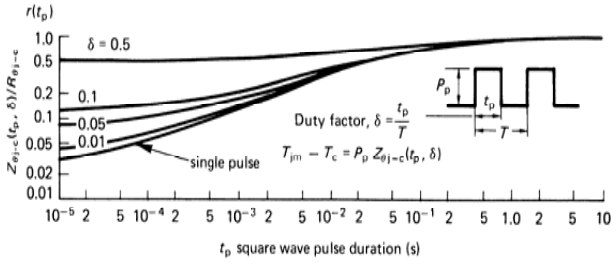


Figure 5.7. *Transient thermal impedance curves; normalised with respect to the steady state thermal resistance, $R_{\theta j\text{-}c}$.*

5.3 Average power dissipation

Two commonly used empirical methods for determining power dissipation P_d are

- graphical integration and
- power superposition.

5.3.1 Graphical integration

Graphical integration may be formulated by digitally storing a complete cycle of test device voltage and current under limiting steady-state temperature conditions. Each voltage and current time-corresponding pair are multiplied together to give instantaneous values of power loss. Numerical integration techniques are then employed to give the average power dissipation.

5.3.2 Practical superposition

This technique is based on substituting a smooth dc voltage source for a complex waveform. A two-pole, two-position switching arrangement is used, which firstly allows operation of the load with the device under test, until the monitored case temperature stabilises. Then, by throwing the switch to the test mode position, the device under test (DUT) is connected to a dc power supply, while the other pole of the switch supplies the normal power to the load to keep it operating at full power level conditions. The dc supply is adjusted so that the semiconductor case temperature remains approximately constant when the switch is thrown to each position for about 10 seconds. The dc source voltage and current values are multiplied together to obtain the average power dissipated.

5.4 Power losses from manufacturers' data sheets

The total power dissipation P_d is the sum of the switching transition loss P_{ss} the on-conduction loss P_{d}, drive input device loss P_G, and the off-state leakage loss P_f.
The average total power loss is given by

$$P_d = f_s \int_0^{1/f_s} v(t)i(t)dt \qquad \text{(W)} \qquad (5.21)$$

where f_s is the switching frequency and *v(t)* and *i(t)* are the device instantaneous voltage and current over one complete cycle of period $1/f_s$. The usual technique for determining total power loss is to evaluate and sum together each of the individual average power loss components.

5.4.1 Switching transition power loss, P_s

Figure 5.8 shows typical power device voltage-current switching waveforms. Normally an exact solution is not required and an approximation based on straight line switching intervals is usually adequate.
For a resistive load, as derived in chapter 6

$$P_s = \tfrac{1}{6} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.22)$$

and for an inductive load, as derived in chapter 6

$$P_s = \tfrac{1}{2} V_s I_m \tau f_s \qquad \text{(W)} \qquad (5.23)$$

where τ is the period of the switching interval (both on and off), and V_s and I_m are the maximum voltage and current levels as shown in figure 5.8. Switching losses occur at both turn-on and turn-off.

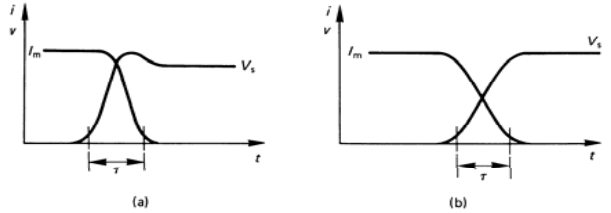


Figure 5.8. *Typical voltage and current at turn-off switching transition for: (a) an inductive load and (b) a resistive load. Current and voltage are interchanged at turn-on.*

5.4.2 Off-state leakage power loss, P_ℓ

During the switched-off period, a small, exponentially temperature dependent current I_ℓ, will flow through the switch. The loss due to this leakage current is

$$P_\ell = I_\ell V_s(1-\delta) \quad \text{(W)} \qquad (5.24)$$

where δ is the on-time duty cycle of the switch. Normally P_ℓ is only a small part of the total loss so that the error in neglecting P_ℓ is not usually significant.

5.4.3 Conduction power loss, P_c

The average conduction power loss under a steady-state current condition is given by

$$P_c = \delta I_{on} V_{on} \quad \text{(W)} \qquad (5.25)$$

although equation (5.21) is valid in the general case when the integration is performed over the interval corresponding to δ.
The conduction loss for the MOSFET is usually expressed in terms of its on-state resistance (equations (3.14) and (4.12))

$$\begin{aligned} P_c &= \delta\, I^2_{d(rms)} R_{ds(on)} \\ &\simeq \delta\, I^2_{d(rms)} R_{ds(on)}(25°\text{C}) \left\{1+\frac{\alpha}{100}\right\}^{T_J-25°\text{C}} \quad \text{(W)} \end{aligned} \qquad (5.26)$$

where α is the temperature coefficient of the on-state resistance, which is positive. A linear resistance approximation of equation (5.26) is quite accurate above 25°C if α is small, such that P_c can be approximated by

$$P_c \approx \delta\, I^2_{d(rms)} R_{ds(on)}(25°\text{C})\{1+\alpha(T_j-25°\text{C})\} \quad \text{(W)} \qquad (5.27)$$

5.4.4 Drive input device power loss, P_G

A portion of the drive power is dissipated in the controlling junction or, in the case of the MOSFET, in the internal gate resistance. Usually more power is dissipated in the actual external drive circuit resistance. Drive input loss is normally small and insignificant compared with other losses, and can usually be ignored.
Two possible exceptions are:

- One notable exception is in the case of the power thyristor, where continuous gate drive is used to avoid loss of latching or when the holding current is high. The holding current can be 3% of the anode current thus the gate to cathode junction loss can be included in the total loss calculation for better accuracy. Thus, for a gate junction voltage V_{GC} the gate losses are given by

$$P_g = \delta\, I_G V_{GC} \qquad (5.28)$$

The recovery loss of the gate commutated thyristor (GCT) cathode junction can be included since it is significant because the full anode current is extracted from the gate, thus is involved in recovery of the cathode junction.

- A second exception is the MOSFET and IGBT at high switching frequencies, >50kHz, when the loss in the device, associated with providing the gate charge Q_T is given by equation (4.35):

$$P_G(R_{\text{int}}) = V_{gg} Q_T f_s \frac{R_{G\text{int}}}{R_{G\text{int}} + R_{G\text{ext}}} \quad \text{(W)} \qquad (5.29)$$

5.5 Heat-sinking design cases

Heat-sink design is essentially the same for all power devices, but the method of determining power loss varies significantly from device type to device type. The information given in data sheets, in conjunction with the appropriate equation in table 5.2, allows the designer to calculate power semiconductor thermal rating for a variety of conditions.
Generally heatsink design is more readily visualised if a thermal equivalent electrical circuit model approach is adopted, as shown in figure 5.1. The examples to follow illustrate the approach.

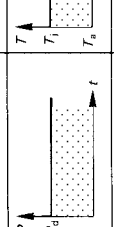
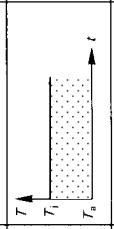
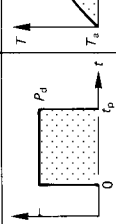
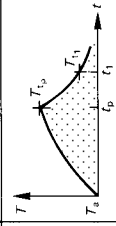
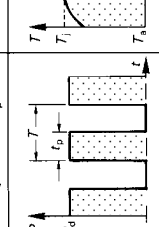
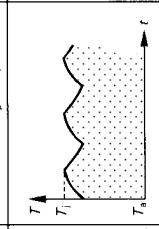
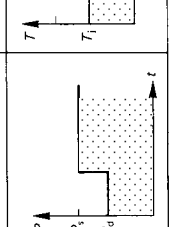
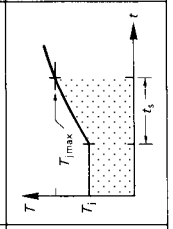
thermal parameter			thermo electric model		
temperature drop	degrees Kelvin	ΔT	potential difference	Volts	V
power dissipated	Watts	P	current flow	Amps	I
thermal resistance	K/W	R_θ	Ohm's resistance	Ohms	R

5.5.1 Heat-sinking for diodes and thyristors

At low switching frequencies (<100 Hz), switching loss can be ignored. In the case of rectifying diodes or converter-grade thyristors, 50 to 60 Hz, switching loss can usually be ignored. Fast-recovery power diodes switching at less than 500Hz can also have switching losses neglected at low VA levels.

5.5.1i - *Low-frequency switching*
At a given current level I_F and on-time duty cycle δ, on-state power loss can be read directly from the manufacturers' data. Figure 5.9a illustrates loss for square-wave power pulses, while figure 5.9b illustrates loss in the case of half-wave sinusoidal current. Figure 5.9b gives energy loss per cycle, which may be converted to power when multiplied by the sinusoidal pulse frequency.
Thyristor loss due to the current waveform initial rate of rise of current, *di/dt*, can be incorporated and its contribution is added into the manufacturers' conduction loss data for a given device type.

Table 5.4. Power rating equations based on thermal considerations

Load condition	Junction power loss waveform	Junction temperature rise waveforms	Junction temperature solution
(a) Continuous			$T_j - T_a = P_d R_\theta$
(b) Single pulse			$T_{t_p} - T_a = P_d z_\theta(t_p),\ \delta = 0$ $T_{t_1} - T_a = P_d\{z_\theta(t_1) - z_\theta(t_1 - t_p)\}$
(c) Constant frequency and duty cycle			$\delta = t_p/T$ approximate steady-state solution $T_j - T_a = P_d\{\delta R_\theta + (1-\delta) z_\theta(T + t_p)$ $- z_\theta(T) + z_\theta(t_p)\}$
(d) Continuous duty followed by a step in power			$T_{j\max} - T_j = P_d R_\theta + (P_s - P_d) z_\theta(t_s)$

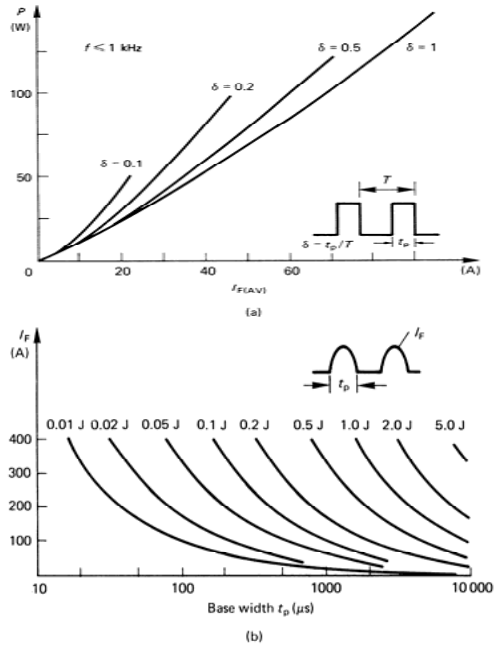


Figure 5.9. *Diode on-state energy loss at low frequency as a function of forward current for: (a) squarewave power pulses and (b) sinusoidal power pulses.*

5.5.1ii - *High-frequency switching*

At frequencies greater than about 100 Hz, fast-recovery diodes are normally employed and at about 500Hz, switching losses must be added to the on-state conduction loss. Diode turn-off loss is usually more significant than turn-on loss. Manufacturers provide maximum reverse recovery charge, Q_R, characteristics as shown in figure 5.10. The reverse recovery charge is a linear function of temperature and between the given junction temperatures of 25°C in figure 5.10a and 150°C in figure 5.10b, interpolation of Q_R is used.

The reverse recovery W.s/pulse, J_R, can be approximated by

$$J_R = V_R Q_R \quad \text{(J)} \qquad (5.30)$$

where V_R is the reverse voltage applied to the diode just after turn-off. The reverse recovery average power loss is given by

$$P_s = V_R Q_R f_s \quad \text{(W)} \qquad (5.31)$$

The total average power loss is the algebraic sum of the steady-state conduction loss and the recovery loss.

Example 5.1: ***Heat-sink design for a diode***

A fast-recovery diode switches 60 A rectangular current pulses at 10 kHz. The off-state bias is 400 V and the external circuit inductance limits the reverse dI_F/dt to 100 A/μs. If the device junction-to-case thermal resistance is 0.7 K/W, calculate the minimum heat-sink requirement with a 50 per cent duty cycle, if the maximum ambient temperature is 40°C.

Solution

The steady-state loss given from figure 5.9a is about 40 W when using $I_{F(AV)} = 30$ A for $\delta = 0.5$.

Minimum heat-sinking requirements occur when T_j is a maximum, that is 150°C from figure 5.10b. From figure 5.10b, for dI_F/dt = 100 A/μs and I_F = 60 A, the maximum reverse recovery charge is 1.3 μC. The switching power loss (over estimate) is given by

$$P_s = Q_R V_R f_s$$
$$= 1.3\mu C \times 400V \times 10kHz = 5.2W$$

The total power loss is therefore

$$P_d = 40 + 5.2 = 45.2W$$

Since the frequency and duty cycle are both high, the concept of thermal resistance is appropriate; that is

$$T_j = T_a + P_d (R_{\theta j\text{-}c} + R_{\theta c\text{-}a})$$

Therefore $$150°C = 40V + 45.2A \times (0.7 + R_{\theta c\text{-}a})$$

whence $$R_{\theta c\text{-}a} = 1.73 \text{ K/W}$$

Figure 5.2b shows that a minimum of 50 mm length of matt black heat sink is required. This assumes that the case-to-sink thermal resistance is negligible. In order to improve device reliability and lifetime, operation at $T_j$max is avoided. A derating of 40 to 50°C significantly reduces junction thermal fatigue and can result in a tenfold improvement in reliability. To restrict $T_j$max to 100°C, $R_{\theta c\text{-}a}$=0.7 K/W, necessitating 120 mm of the

heat sink as characterised in figure 5.2b. The flatness of the $R_{\theta s\text{-}a}$ curve means that the effectiveness of the heat sink is diminished and a shorter length of a profile offering lower thermal resistance would be more effective in reducing device thermal fatigue.

♣

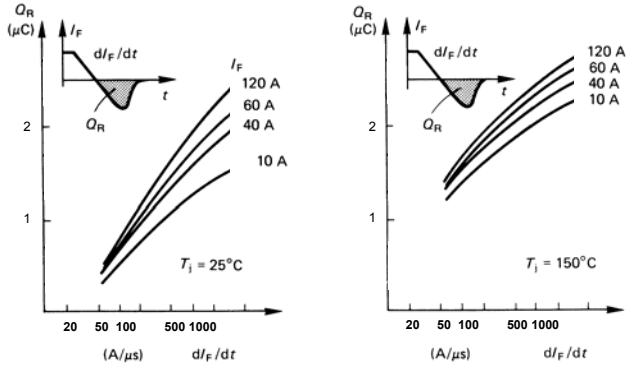


Figure 5.10. Reverse recovery charge as a function of forward current and dI_F/dt at: (a) 25°C and (b) 150°C junction temperature.

5.5.2 Heat-sinking for IGBTs

The IGBT conduction loss is related to the gate voltage and the collector current magnitude, which specify the on-state voltage. No simple power loss characteristic is possible, as in figure 5.9 for the diode and thyristor. Fortunately, the power switching IGBT is used in such a way that its on-state collector-emitter voltage is fairly constant, whence conduction loss is given by

$$P_c = \delta \, v_{ce} \bar{I}_c \quad \text{(W)} \qquad (5.32)$$

Example 5.2: ***Heat-sink design for an IGBT- repetitive operation at a high duty cycle***

A power IGBT is used to switch a 20 A, 100 V highly inductive load at 10 kHz. The transistor maximum on-state duty cycle is 90 per cent and the device has a junction-to-case thermal resistance of 0.7 K/W. The transistor on-state voltage is maintained at 2 V

and the switch-on and switch-off times are 1 and 2 μs respectively. If the junction temperature is not to exceed 125°C with a maximum ambient temperature of 35°C, what is the minimum heat-sink requirement? Assume that the transistor is in a T0247 package, which is mounted directly on the heat sink but with silicone grease used.

Solution

Since both the duty cycle and switching frequency are high, the peak junction temperature is closely approximated by the average junction temperature. That is, the concept of thermal resistance is valid.

The on-state power loss is given by

$$P_c = \delta v_{ce} \bar{I}_c$$
$$= 0.9 \times 2\text{V} \times 20\text{A} = 36\text{ W}$$

From equation (5.23), the switching losses for an inductive load are

$$P_s = P_{s(\text{on})} + P_{s(\text{off})}$$
$$\tfrac{1}{2} \times 100 \times 20 \times (1\mu\text{s} + 2\mu\text{s}) \times 10\text{ kHz} = 30\text{ W}$$

Total power losses P_d are 36W+30W = 64 W.

From

$$T_{j\max} = T_a + P_d(R_{\theta j\text{-c}} + R_{\theta c\text{-s}} + R_{\theta s\text{-a}})$$
$$125°\text{C} = 35°\text{C} + 64\text{W} \times (0.7 + 0.1 + R_{\theta s\text{-a}})$$

Therefore $R_{\theta c\text{-a}} = 0.53$ K/W

The case-to-heat-sink thermal resistance value of 0.1 K/W for a T0247 non-insulated case using silicone thermal grease was obtained from table 5.1. To obtain the minimum heat-sink thermal resistance of 0.53 K/W, 150 mm of the heat sink with cross-section shown in figure 5.2a is required. Clearly a sink profile that has a lower thermal resistance per unit length would be more suitable.

♣

5.5.3 Heat-sinking for power MOSFETs

Switching losses in MOSFETs tend to be low at frequencies below 20 kHz and therefore may be neglected, along with gate and off-state losses. Conduction loss is generally expressed in terms of the on-state resistance as I^2R loss. The first step in the thermal design is to determine the total power dissipation in the device, which is generally dominated by the conduction loss. Determination of this loss is not trivial since, while the power dissipation determines junction temperature, the power dissipation itself is a function of junction temperature, because the on-state resistance increases with temperature, as shown in figure 3.13.

Example 5.3: ***Heat-sink for a MOSFET - repetitive operation at high peak current, low duty cycle***

Find the thermal resistance of the heat sink needed for a MOSFET conducting a repetitive 20 A rectangular current waveform. On-time is 10 μs, duty cycle is 0.1 per cent and the maximum ambient temperature is 40°C. Assume $R_{ds(\text{on})}$ at 150°C and 20 A is 5 Ohms, and $R_{\theta j\text{-c}} = 1.5$ K/W.

Solution

Since the on-state duty cycle and switching frequency are both low, the peak junction temperature at the end of the on-period will be significantly different from the average junction temperature. The concept of thermal resistance from junction to case is therefore invalid; the concept of thermal impedance is used instead.

The power per pulse = $P_p = I^2R = 20^2 \times 5\Omega = 2 \times 10^3$ W

The case temperature is given by

$$T_j = T_c + P_p \times Z_{\theta j\text{-c}}$$
$$= T_c + P_p\, r(t_p)\, R_{\theta j\text{-c}}$$

where $r(t_p)$ is the transient thermal impedance factor for the junction-to-case. For a 10 μs pulse from figure 5.7, $r(t_p) = 0.03$, assuming δ=0.001≈ a single pulse condition, thus

$$150°\text{C} = T_c + 2 \times 10^3 \times 0.03 \times 1.5$$

that is $T_c = 60°\text{C}$

Because of the heat-sink thermal inertia, the concept of thermal resistance is used for calculations involving the heatsink. That is

$$T_c = T_a + \bar{P}_d R_{\theta c\text{-a}} = T_a + \delta P_d R_{\theta c\text{-a}}$$
$$60°\text{C} = 40°\text{C} + 0.001 \times 2 \times 10^3 \times R_{\theta c\text{-a}}$$

thus $R_{\theta c\text{-a}} = 10$ K/W

The heat sink of cross-section shown in figure 5.2a is not suitable in this application, and one of a much smaller surface area is applicable. A heatsink may not be necessary since the package thermal resistance $R_{\theta c\text{-a}}$, shown in figure 5.1, may be less than 10K/W, there in satisfying equation (5.12). See problem 5.4.

♣

If the junction operating temperature is unknown but can be assumed greater than 25°C, from equation (5.27), the total power loss can be expressed as

$$P_d = P_o + I_{d(\text{rms})}^2 R_{ds(\text{on})}(25°\text{C})\left\{1 + \alpha (T_j - 25°\text{C})\right\} \quad \text{(W)} \qquad (5.33)$$

where P_o represents all losses other than the conduction loss, and is assumed

temperature independent The temperature coefficient α for $R_{ds(on)}(25°C)$ is positive, typically 1 per cent/K as indicated in figure 3.13. The usual thermal equality holds, that is

$$T_j = T_a + R_{\theta j\text{-a}} P_d \quad \text{(K)} \qquad (5.34)$$

Combining equations (5.33) and (5.34) by eliminating T_j yields

$$P_d = \frac{P_o + I_{d(\text{rms})}^2 R_{ds(\text{on})}(25°C)\{1+\alpha(T_a - 25°C)\}}{1 - I_{d(\text{rms})}^2 R_{ds(\text{on})}(25°C)\alpha R_{\theta j\text{-a}}} \quad \text{(W)} \qquad (5.35)$$

The denominator yields an asymptotic maximum drain current of

$$I_{d(\text{rms})} = \frac{1}{\sqrt{R_{ds(\text{on})}(25°C)\ \alpha\ R_{\theta j\text{-c}}}} \quad \text{(A)} \qquad (5.36)$$

at which current thermal runaway would result. In practice, insufficient gate voltage is available and the device would leave the constant-resistance region and enter the constant-current region, where the above analysis is invalid.

Example 5.4: ***Heat-sink design for a MOSFET -repetitive operation at high duty cycle***

A power MOSFET switches 5 A rms at 10 kHz with a maximum on-state duty cycle of 90 per cent. The junction-to-case thermal resistance is 0.7 K/W, the maximum ambient temperature 35°C, and on-state resistance at 25°C is 1 Ohm. If the heat-sink arrangement yields an effective case-to-ambient thermal resistance of 1.3 K/W and α=0.01 /K, what is the junction operating temperature?

Solution

Since the switching frequency and duty cycle are both relatively high, the thermal resistance concept based on average junction power dissipation is valid.

Assuming zero losses other than conduction losses, then $P_o = 0$. Equations (5.33) and (5.34) rearranged to eliminate P_d yielding

$$T_j = \frac{T_a + R_{\theta j\text{-a}} I_{d(\text{rms})}^2 R_{ds(\text{on})}(25°C)\{1 - 25\alpha\}}{1 - \alpha R_{\theta j\text{-a}} I_{d(\text{rms})}^2 R_{ds(\text{on})}(25°C)} \quad \text{(W)} \qquad (5.37)$$

Assuming typical $\alpha = 0.01$/K and $R_{\theta j\text{-a}} = R_{\theta j\text{-c}} + R_{\theta c\text{-a}}$

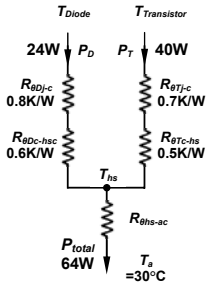
$$T_j = \frac{35°C + 2 \times 5^2 \times 1\Omega \times (1 - 25 \times 0.01)}{1 - 0.01 \times 2 \times 5^2 \times 1\Omega} = 145°C$$

♣

Example 5.5: ***Two thermal elements on a common heatsink***

A dc chopper has a MOSFET switch that dissipates 40W and a load freewheel diode that dissipates 24W. Each power device is mounted on a common heatsink. The MOSFET has a junction-to-case thermal resistance of 0.7K/W and a case-to-heatsink thermal resistance of 0.5K/W. The diode has a junction-to-case thermal resistance of 0.8K/W and a case-to-heatsink thermal resistance of 0.6K/W.

i. Determine the maximum heatsink thermal resistance that maintains both junction temperatures below 90°C in a 30°C ambient.
ii. Semiconductor lifetime approximately doubles for every 10°C decrease in junction temperature. If the heatsink in the previous case is fan cooled, estimate the lifetime improvement if the heatsink thermal impedance is halved with fan cooling.
iii. If the load current is constant (25A) and the switch and diode on-state voltages are the same, determine the chopper on-time duty cycle and device instantaneous losses assuming no switching losses (only on-state losses).



Solution

i. Applying Kirchhoff's voltage law to each loop of the equivalent thermal circuit shown gives:

$$T_{Dj} - T_{hs} = 20\text{W} \times (0.8\text{K/W} + 0.6\text{K/W}) = 28°C$$

$$T_{Tj} - T_{hs} = 40\text{W} \times (0.7\text{K/W} + 0.5\text{K/W}) = 48°C$$

Since both semiconductor devices are mounted on the same heatsink, T_{hs} is the same in each case, the MOSFET virtual junction will operate 20°C hotter than the diode junction. Therefore the MOSFET junction temperature should not exceed 90°C, that is

$$90°C - T_{hs} = 40\text{W} \times (0.7\text{K/W} + 0.5\text{K/W}) = 48°C$$

giving a heat sink surface temperature of 90°C - 48°C = 42°C and a diode junction temperature of 42°C + 28°C = 70°C. The heatsink thermal resistance requirement is

$$T_{hs} - T_a = 42°C - 30°C = R_{\theta hs-a} \times (40\text{W} + 24\text{W})$$

$$R_{\theta hs-a} = 42°C - 30°C \,/\, 40\text{W} + 24\text{W} = 12°C \,/\, 64\text{W} = 0.19\text{K/W}$$

ii. Assume device losses are not affected by temperature and the heatsink thermal resistance is decrease to ½×0.19=0.095K/W, then

$$T_{hs} - T_a = T_{hs} - 30°C = 0.095\text{K/W} \times (40\text{W} + 24\text{W})$$

$$T_{hs} = 0.095\text{K/W} \times (40\text{W} + 24\text{W}) + 30°C = 36.1°C$$

The device junction temperatures are given by

$$T_{Dj} - 36.1°\text{C} = 20\text{W} \times (0.8\text{K/W} + 0.6\text{K/W}) \text{ that is } T_{Dj} = 64.1°\text{C}$$

$$T_{Tj} - 36.1°\text{C} = 40\text{W} \times (0.7\text{K/W} + 0.5\text{K/W}) \text{ that is } T_{Tj} = 84.1°\text{C}$$

The junction temperature of each device has decreased by about 6°C, so although the lifetime will have increased, lifetime improvement is not doubled. Device package thermal properties are more dominant than the heatsink in determining junction temperatures.

iii. If the on-state duty cycle is δ and the instantaneous device losses are P (and the same since on-state voltage is the same for both devices and the current is constant hence the same when each device is conducting) then

$$\text{mosfet} \quad \delta P = 40\text{W}$$

$$\text{diode} \quad (1-\delta) P = 24\text{W}$$

Summing these two equations gives an instantaneous loss of $P = 64$W, whence a switch on-state duty cycle of $\delta = ⅝$, that is the switch conducts for 62½% of the cycle period. The diode on-state voltage is therefore 64W/30A= 2.13V and the MOSFET on-state resistance is $64\text{W}/30\text{A}^2 = 71\text{m}\Omega$.

♣

Example 5.6: ***Six thermal elements in a common package***

A three phase full-wave diode rectifier package consists of six diode die within a single module. The junction-to-case thermal resistance of each die is 0.24K/W. The module is mounted on a heatsink with a module-to-heatsink contact thermal resistance of 0.2K/W and a heatsink-to-ambient thermal resistance of 0.1K/W. The maximum ambient temperature is 30°C and high inductive load current is constant at 100A. If the diode on-state voltage is 1V, determine

i. the diode junction temperature
ii. current to double the rectifier lifetime (decrease junction temperature by 10°C
iii. the heatsink to double the rectifier lifetime (at 100A).

Solution

i. During rectification two diodes always conduct therefore total module conduction losses are

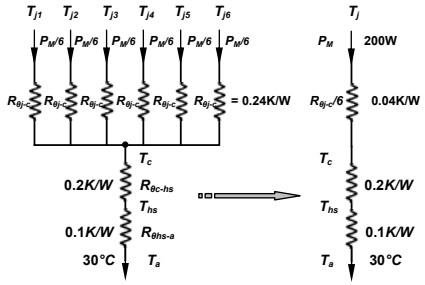
$$P_M = 2 \times I_o \times V_{Don} = 2 \times 100\text{A} \times 1\text{V} = 200\text{W}$$

The figure shows how the six thermal paths can be reduced to the simplified equivalent thermal model on the right.

Applying Kirchhoff's voltage law

$$T_j - T_a = P_M \times (⅙ R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a})$$

$$T_j - 30°\text{C} = 200\text{W} \times (⅙ \times 0.24\text{K/W} + 0.2\text{K/W} + 0.1\text{K/W}) \quad \Rightarrow \quad T_j = 98°\text{C}$$



ii. If the current is to reduce so as to decrease the diode junction temperature by 10°C then

$$T_j - T_a = P_M \times (⅙ R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a})$$

$$88°\text{C} - 30°\text{C} = P_M \times (⅙ \times 0.24\text{K/W} + 0.2\text{K/W} + 0.1\text{K/W}) \quad \Rightarrow \quad P_M = 170.6\text{W}$$

Assuming the diode on-state voltage drop is independent of current, that is remains 1V then

$$P_M = 2 \times I_o \times V_{Don}$$

$$170.6\text{W} = 2 \times I_o \times 1\text{V} \quad \Rightarrow \quad I_o = 85.3\text{A}$$

iii. When the junction temperature is reduced by 10°C to 88°C by decreasing the heatsink thermal resistance, and the constant load current is maintained at 100A

$$T_j - T_a = P_M \times (⅙ R_{\theta j-c} + R_{\theta c-hs} + R_{\theta hs-a})$$

$$88°\text{C} - 30°\text{C} = 200\text{W} \times (0.04\text{K/W} + 0.2\text{K/W} + R_{\theta hs-a}) \quad \Rightarrow \quad R_{\theta hs-a} = 0.5\text{K/W}$$

♣

Reading list

Fishenden, M. and Saunders, 0. A., *An Introduction to Heat Transfer,* Oxford University Press, 1982.

Problems

5.1. A thyristor bridge switches at 1 kHz and the total energy losses per thyristor are 0.01 Joule per cycle. The thyristors have isolated studs and a thermal resistance of 2 K/W. The heat sink has a thermal resistance of 1.8 K/W. Calculate the maximum number of thyristors that can be mounted on one heat sink if the thyristor junction temperature is not to exceed 125°C in an ambient of 40°C. What is the heat sink temperature?

[3 devices, T_s = 94°C]

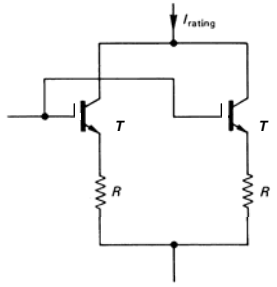


Figure 5.11. *Problem 5.2.*

5.2. A transistorised switch consists of two IGBTs and two 1 Ohm current-sharing resistors, as shown in figure 5.11, mounted on a common heat-sink. Each transistor has a thermal resistance $R_{\theta j\text{-hs}}$ of 2 K/W, while each resistor has a thermal resistance $R_{\theta r\text{-hs}}$ of 1 K/W. The maximum switching frequency is 1 kHz and the maximum duty cycle is 99.99 per cent. The heat-sink thermal resistance $R_{\theta hs\text{-a}}$ is 1 K/W. The energy losses per transistor are 5 mJ/A per cycle. If the ambient temperature is 30°C, maximum allowable junction temperature is 150°C, and the maximum allowable resistor internal temperature is 100°C, calculate the switch maximum current rating based on thermal considerations. What are the operating temperatures of the various components, assuming ideal current sharing?

[6.88 A, T_r = 100°C, T_{hs} = 88°C, T_j = 122.5°C]

5.3. Figure 5.12a shows the circuit diagram for a power current sink which utilises a 40V source. Both the IGBTs *T* and wire wound resistors *R* are mounted on a common heat-sink, of thermal resistance $R_{\theta hs\text{-a}}$ = 1 K/W. The transistor has a thermal resistance of 2 K/W from the junction to the heat-sink, and 10 K/W from the junction to air via the transistor casing exposed to the air. The resistor has a mounting thermal resistance from the insulated wire to the heat-sink of 1 K/W and 10 K/W from the wire to the air via its casing exposed to the air. The maximum transistor junction temperature is 423

K, the maximum resistor wire temperature is 358 K and the ambient air temperature is 303 K.

Based on thermal considerations, what is the maximum current rating of the current sink and under such conditions, what is the heat-sink temperature?

What power rating would you suggest for the 1 Ohm current measurement resistor?

Are there any difficulties in operating the transistor in the linear region in this application if it is in a 120 W dissipation package which is derated according to figure 5.12b?

[1.36 A, 69°C, > 2 W]

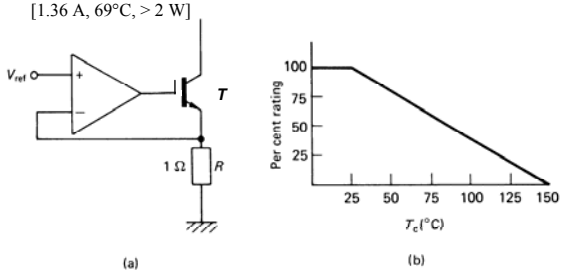


Figure 5.12. *Problem 5.3.*

5.4. A power IGBT switches a 600 V, 25 A inductive load at 100 kHz with a 50 per cent on-time duty cycle. Turn-on and turn-off both occur in 100 ns and the collector on-state voltage is to be 2 V.

Calculate the total power losses, P_d, of the switch.

The switch has a thermal resistance $R_{\theta j\text{-hs}}$ = 0.05 K/W, and the water-cooled heatsink provides a thermal resistance $R_{\theta hs\text{-w}}$ = 0.05 K/W. Calculate the operating junction temperature if the water for cooling is maintained at 35°C.

The 25 A steady state load current is stepped to 200 A. Calculate the surge power dissipation P_s, at 200 A, assuming transistor switching and on-state characteristics remain unchanged.

The junction temperature for a power surge during steady-state operation is given by case (d) in table 5.2.

With the aid of figure 5.7, determine the junction temperature at the end of a 0.1s, 200 A pulse. How long is it before the junction temperature reaches $T_{j\max}$ = 125°C, with a collector current of 200 A? (Assume $R_{\theta c\text{-hs}}$ =0).

[175 W, 52.5°C, 1400 W, 112.6°C, 0.5 s]

5.5 Rework example 5.4, finding the case temperature when the switching losses equal the on-state loss.