Driving Transistors and Thyristors

The thyristor, being a multiple (three) bipolar junction device, is essentially a current-controlled device. As illustrated in figure 7.1a, a current must be supplied between the gate and cathode terminals to produce cathode injection, hence anode current flow, provided the anode is forward biased. The magnitude of gate drive current determines the delay time and the anode current rise time. In gate commutated thyristors, a negative gate current must be produced, the magnitude determining the turn-off delay time and anode current fall time.

The power MOSFET and IGBT are voltage controlled devices with turn-on and turn-off requirements fundamentally different to bipolar devices. With the n-channel enhancement-mode power MOSFET and IGBT, a positive voltage must be applied between the gate and source terminals to enhance a channel which allows a drain current, if the drain is positively biased with respect to the source, as shown in figure 7.1b. Generally the MOSFET and IGBT are easier to drive than the bipolar thyristor, and only a few basic considerations are required for MOSFET and IGBT gate circuit implementation.

Figure 7.1. Thyristor and transistor drive requirements:
(a) current drive for the bipolar junction thyristor and (b) voltage drive for the MOSFET and IGBT.

7.1 Application of the power MOSFET and IGBT

The MOSFET gate is isolated electrically from the source by a dielectric layer of silicon dioxide. Theoretically no current flows into the gate when a dc voltage is applied to it. In practice, gate current is required to charge device capacitances and a small leakage current of the order of nano-amps does flow in order to maintain the gate voltage.

When no voltage is applied between the gate and source terminals (but with zero impedance), the drain-to-source impedance is very high and only a small leakage current of less than a milli-amp flows in the drain, until the applied voltage exceeds the drain-to-source avalanche voltage, \( V_{DSS} \).

When a positive gate voltage is applied, an electric field is produced which modulates the drain-to-source resistance. When a gate voltage exceeds the threshold voltage level the channel resistance reduces to a low resistance and drain current flows. The maximum drain current depends on the gate voltage magnitude, assuming that the impedance of the external drain circuit is not current-limiting.

\[
\begin{align*}
&15V-30V \\
&HCPL3210 \\
&dv/dt=15kV/\mu s \\
&\text{I}_{o}=\pm2A
\end{align*}
\]

Turn off - reducing the drain current to the leakage current level - is achieved by reducing the gate voltage to below the gate threshold voltage level. The drain switching speeds are essentially determined by that speed at which the gate voltage can reach a level above the threshold voltage (for turn-on) or below the threshold voltage (for turn-off). Although the gate-to-source capacitance is an important parameter, the gate-to-drain capacitance is more significant because of the Miller effect, as considered in section 4.4.2. During switching, the dynamic gate-to-drain capacitance can be effectively much larger than the gate-to-source capacitance. The Miller capacitance typically requires more charge for switching than the gate-to-source capacitance.
MOSFETs can also be driven directly from ttl gates. Table 7.2 shows ttl typical current source and sink capabilities and switching speeds. Low supply voltage, typically 5V, and high internal sourcing impedance characteristics restrict MOSFET switch-on speed and gate voltage level. The ttl sink capability is significantly higher than source capability, hence a pull-up resistor as shown in figure 7.2c enables the sinking capability to be exploited at turn-on, as well as at turn off. A limitation of using ttl for driving MOSFETs is that the gate voltage is restricted to less than 5V, hence if the drain current is not to be restricted, low gate threshold voltage trench gate MOSFETs and IGBTs are used. An open collector ttl drive technique as shown in figure 7.2d overcomes the gate voltage limitation as well as improving the current source limit.

Very fast switching speeds are attained with the capacitive driver shown in figure 7.2e. Such drivers can both source and sink typically 1.5 A in tens of nanoseconds. An isolated gate-to-source drive version is shown in figure 7.2f, where a floating 15 V rail is used and the gate control signal is optically transmitted with high dv/dt capability. The driver incorporates high current output, with modest propagation delays.

Figure 7.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the 4049 source-to-sink output characteristics in figure 7.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 7.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.

In figure 7.2b the gate drive current is the output current of the cmos gate multiplied by the gain β of the bipolar transistors. No bipolar saturation times are incurred since the transistors are operating as emitter followers, which cannot saturate. The operating frequency is no longer restricted by the cmos output current limitations.

Figure 7.2. Gate drive circuits for the MOSFET and IGBT:
(a) driven from cmos; (b) driven from cmos and an emitter follower; (c) driven from ttl with pull-up resistor which increases sourcing capability; (d) driven from open collector ttl with an external current source; (e) driven from a high-current cmos clock driver; (f) opto-isolated driver circuit; (g) drive circuits for a totem pole connected p and n-channel MOSFET leg; (h) driven from a pulse transformer; and (i) fibre optic translation stage.

7.1.1 Gate drive circuits

The trench gate n-channel enhancement-mode power MOSFET (or IGBT) with a low threshold voltage interfaces easily with logic level integrated circuits. This allows low-power digital logic circuits to control directly high-power levels. Figure 7.2 shows a series of ttl and cmos circuits driving power MOSFETs, each circuit offering different levels of switching speed and performance.

When driving a MOSFET directly from a cmos gate output, as shown in figure 7.2a, only modest rise and fall times can be expected because of the limited source and sink current available from a cmos gate. Figure 7.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the 4049 source-to-sink output characteristics in figure 7.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 7.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.

If shorter delays and faster drain rise and fall times are required there are several ways to obtain them. The simplest is to parallel a number of identical cmos inputs and outputs as shown dotted in figure 7.2a. Each circuit offering different levels of switching speed and performance.

Drive circuits for p-channel MOSFETs may be complicated by the reference signal voltage level, as shown in the series n and p-channel totem pole in figure 7.2g. Figure 7.3a illustrates the output configuration of a typical cmos output stage, which consists of a series-connected p and n-channel MOSFET with the gates connected together. The cmos totem pole output stage is driven by a common signal, hence the name complementary mos - cmos - and when the input is high the n-channel device is on and the p-channel off, while when the input is low, the p-channel turns on and the n-channel turns off. However, cmos has a limited current output capability as shown in the 4049 source-to-sink output characteristics in figure 7.3b and c. The cmos gate output has to drive as a load the power MOSFET capacitive gate. In this configuration, the turn-on current is supplied from the p-channel fet, which has the poorer characteristics of the cmos pair. The turn-off current is sunk by the n-channel fet. Table 7.1 shows cmos typical current source and sink capabilities, switching speeds, and output impedance. It will be seen that the best performance, by far, is achieved from the 4049 and 4050 buffers.

In figure 7.2b the gate drive current is the output current of the cmos gate multiplied by the gain β of the bipolar transistors. No bipolar saturation times are incurred since the transistors are operating as emitter followers, which cannot saturate. The operating frequency is no longer restricted by the cmos output current limitations.

Figure 7.3. CMOS 4049 inverter output: (a) output cmos totem pole; (b) p-channel drain sourcing; and (c) n-channel drain sinking, both at 25°C.
A simple method of driving an n-channel MOSFET, with its source not referenced to ground, is shown in figure 7.2h. Electrical (galvanic) isolation is achieved by means of a pulse transformer. The internal parasitic diode in Q1 provides the path for the n-channel MOSFET gate to charge. When the pulse transformer saturates, Q1 blocks any discharge of the gate until turn-off, when a negative transformer pulse turns on Q1, thereby discharging the n-channel gate charge.

An alternative translation method using a fibre optic stage is shown in figure 7.2i. The temperature-independent, high threshold characteristics of 74AC technology is used for a simple detector comparator. A Schmitt input (hysteresis) gate (74AC132) improves noise immunity.

In general, translation from ttl levels can be achieved with Zener diode bias circuits.

Table 7.3: Gate driver summary

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Isolated Isolation Voltage</th>
<th>Operating Supply Voltage</th>
<th>On speed (typical)</th>
<th>Off speed (typical)</th>
<th>Output Peak Sink Current (Au)</th>
<th>Output Peak Source Current (Au)</th>
<th>Input Signal Compatibility</th>
<th>Output Channels</th>
<th>Types</th>
</tr>
</thead>
<tbody>
<tr>
<td>FAN3278</td>
<td>No</td>
<td>na</td>
<td>8V - 27V</td>
<td>17</td>
<td>8</td>
<td>35</td>
<td>1</td>
<td>1.5</td>
<td>TTL</td>
</tr>
<tr>
<td>FAN3121/3122</td>
<td>No</td>
<td>4.5V - 18V</td>
<td>23</td>
<td>23</td>
<td>23</td>
<td>11.4</td>
<td>10.6</td>
<td>TTL/CMOS</td>
<td>1 Low-side</td>
</tr>
<tr>
<td>FAN73711</td>
<td>No</td>
<td>10V - 20V</td>
<td>25</td>
<td>150</td>
<td>15</td>
<td>150</td>
<td>4</td>
<td>4</td>
<td>TTL</td>
</tr>
<tr>
<td>FAN7900-F055</td>
<td>No</td>
<td>10V - 22V</td>
<td>25</td>
<td>140</td>
<td>20</td>
<td>140</td>
<td>4.5</td>
<td>4.5</td>
<td>TTL</td>
</tr>
<tr>
<td>IRS21850S</td>
<td>No</td>
<td>10V - 20V</td>
<td>15</td>
<td>160</td>
<td>15</td>
<td>160</td>
<td>4</td>
<td>4</td>
<td>CMOS/LSTTL</td>
</tr>
<tr>
<td>IRS2186</td>
<td>No</td>
<td>10V - 20V</td>
<td>22</td>
<td>170</td>
<td>18</td>
<td>170</td>
<td>4</td>
<td>4</td>
<td>TTL</td>
</tr>
<tr>
<td>ELT1585</td>
<td>No</td>
<td>4.5V - 12V</td>
<td>12</td>
<td>22</td>
<td>12</td>
<td>22.5</td>
<td>12</td>
<td>12</td>
<td>TTL</td>
</tr>
<tr>
<td>ISL6700</td>
<td>No</td>
<td>9V - 15V</td>
<td>5</td>
<td>45</td>
<td>5</td>
<td>75</td>
<td>1.3</td>
<td>1.4</td>
<td>High and low-side</td>
</tr>
<tr>
<td>IXDD414</td>
<td>No</td>
<td>4.5V - 35V</td>
<td>25</td>
<td>30</td>
<td>22</td>
<td>31</td>
<td>14</td>
<td>14</td>
<td>TTL/CMOS</td>
</tr>
<tr>
<td>ACPL3333J</td>
<td>Yes</td>
<td>3.75V</td>
<td>15V - 30V</td>
<td>50</td>
<td>180</td>
<td>50</td>
<td>2.5</td>
<td>2.5</td>
<td>Input current limit: 12mA</td>
</tr>
<tr>
<td>ACNW3390</td>
<td>Yes</td>
<td>5V</td>
<td>15V - 30V</td>
<td>100</td>
<td>300</td>
<td>100</td>
<td>5</td>
<td>5</td>
<td>Input current limit: 25mA</td>
</tr>
<tr>
<td>PC929L00NS079</td>
<td>Yes</td>
<td>5V</td>
<td>15V - 30V</td>
<td>100</td>
<td>300</td>
<td>100</td>
<td>2.5</td>
<td>2.5</td>
<td>Input current limit: 25mA</td>
</tr>
</tbody>
</table>

From the circuits in figure 7.2 it is seen that there are two basic types of gate drives.

- **Low-side**
- **High-side**

Essentially a low-side driver is one where the control signal and the power device gate are at almost the same potential. The lower switches in bridge legs normally use low-side drivers, while the upper switches require high-side drivers which translate the control signal and gate power to a different potential. The gate drive circuits 7.2a to 7.2e are basic low-side gate drive circuits. The high-side drivers in figures 7.2f to 7.2i translate the control signal to the gate level.

Although the gate drive circuits in figures 7.2a to 7.2i translate the control signal to the device gate, these circuits do not address two important gate drive issues.

- The derivation of the gate drive supply, particularly for floating gate drivers as encountered in inverters.
- The derivation of negative gate bias at turn-off for better immunity to false turn-on due to noise and induced Miller charging effects.

### 7.1.1i - Negative gate drive

The gate drive circuits shown in figure 7.2 only clamp the gate to near zero volts during the off period. The lower bridge leg switch in figure 7.4 uses ±15V gate voltages. The complementary buffers drive the gate-source of the shown device in an H-bridge configuration. The buffers require an isolated 15V dc supply. Since the 15V dc supply is isolated, the complementary buffers can be used for high side gate drives, provided the control signal is isolated, as in figure 7.2. Practically a negative gate bias of -5V is
sufficient for noise immunity while any voltage in excess of this unnecessarily increases turn-on delay and increases gate power requirements. Manufacturers are continually improving power device properties and characteristics. Gate threshold voltage levels are constantly being decreased, and coupled with the fact that the threshold voltage decreases with temperature, negative voltage gate drive is necessary for high noise immunity to prevent false turn-on with high power devices. Gate capacitance improves noise immunity.

7.1.1ii - Floating power supplies

There are three basic methods for deriving floating power supplies for gate drives.

- A low inter-winding capacitance, high-frequency transformer
- A capacitive coupled charge pump
- A diode bootstrap

The upper bridge leg switch T_u in figure 7.4 uses both a diode bootstrap via D_{bs} and a single ended capacitor charge pump via C_{cp}, in order to derive gate power.

1 - capacitive coupled charge pump

By switching T_{cp} at high frequency the low-capacitance, high-voltage capacitor C_{cp} is successively charged through D_{cp1} and discharged through D_{cp}. Discharge through D_{cp} involves charging C_{gs}, the gate voltage supply capacitor. The shown charge and discharge paths both rely on either the upper switch T_u or diode D_u being in a conducting state.

2 - diode bootstrap

When the lower switch T_{lb} or diode D_{l} conduct, high voltage diode D_{bs} allows the upper gate supply capacitor C_{gs} to charge from a 15V dc supply which is referenced to the 0V dc rail. When the upper switch or diode conduct, the bootstrap diode is reverse bias and supports V_{gs} = V_{supply}. Start-up is a problem since the gate of the upper switch T_u is in a high impedance state while its supply is being charged after the lower switch is turned on. For this reason, the bootstrap is usually used in conjunction with a capacitor charge pump.

The only foolproof method to ensure gate power at all times, particularly at start-up and during prolong on-state periods, is to use a high-frequency (power and/or signal) transformer approach.

7.1.2 Gate drive design procedure

The effective gate to source capacitance, C_{gs}, can be calculated from

\[
C_{gs} = \frac{\partial Q_g}{\partial V_g}
\]

where \( R_g \) is the gate equivalent series resistance and \( V_{g1} = V_{TH} \).

The initial slope of the charge in figure 7.5a, 740 pF, is due to the gate source capacitance charging below the gate threshold level. The next charge section between \( Q_{g1} \) and \( Q_{g2} \) in figure 7.5c is due to the Miller effect. The horizontal charge portion is due to the very high drain-source depletion field capacitance as the drain falls below the gate voltage level.

The drain switching times, similar to those derived in 4.4.2, can be calculated from the charge transfer characteristics in figure 7.5, using the following equations.

(i) From figure 7.5c, for turn-on

\[
t_{on} = \frac{Q_{g2}}{\frac{V_{gs}}{V_{gs} + V_{gs}}} \left( \frac{V_{gs} + V_{gs}}{V_{gs}} \right)
\]

(ii) From figure 7.5d, for turn-off

\[
t_{off} = \frac{Q_{g2}}{\frac{V_{gs}}{V_{gs} - V_{gs}}} \left( \frac{V_{gs} - V_{gs}}{V_{gs}} \right)
\]

where \( R_g \) is the gate equivalent series resistance and \( V_{gs} = V_{DH} \).
The energy required for switching is given by
\[ W = Q_g V_g^2 \]  
which is dependent on the drain current and voltage. The gate drive power requirements are given by
\[ P = Q_g V_g i_g \]  
Obviously the faster the switching speed requirement, the higher and faster the gate drive current delivery necessary.

If only 15 mA is available for gate drive then, based on figure 7.5, switching occurs in about 1 µs (from \( Q = 7\)). This level of performance could be expected with circuit 7.2a, and slower switching for the circuit in figure 7.2c. By employing the gate drive in figure 7.2c, the gate voltage is limited to 5 V, hence the MOSFET represented by figure 7.5 could not be switched. The circuits in figures 7.2b and 7.2d are capable of delivering about 100 mA, which yields switching speeds of the order of 150 ns, with only 50 mW of drive power dissipation at 100 kHz. The drive circuit in figure 7.2e is capable of delivering ±1.5 A. Hence the device characterised by figure 7.5 can be switched in only 10 ns.

Switching times deteriorate slightly if reverse gate-to-source biasing is used for higher noise immunity in the off-state. Analysis of the increase in turn-on delay as a result of the use of negative gate drive is presented in Appendix 4.8.

**Example 7.1:** MOSFET input capacitance and switching times

A MOSFET switching a resistive load has the following circuit parameters:
\[ R_s = 47\Omega, \quad R_2 = 100\Omega \]
\[ V_{ds} = 10\text{ V}, \quad V_g^c = 400\text{ V} \]

Based on the charge transfer characteristics in figure 7.5, calculate the gate input capacitance and switching times for MOSFET turn-on and turn-off.

**Solution**

The charge transfer characteristics shown in figure 7.5 are valid for a 100 Ω resistive load and a 10-10 V gate voltage. A 400 V drain switching characteristic is shown.

At turn-on, from figure 7.5a and using equations (7.2) and (7.3)

(i) \( C_n = C_r = Q_{g1}/V_{g1} = 4.4\text{ nC}/6\text{ V} = 740\text{ pF} \)

(ii) \( C_n = 3\text{ nF} \)

At turn-off, from figure 7.5b and using equations (7.4) and (7.5)

(i) \( C_n = (Q_{g2} - Q_{g1})/(V_{g2'} - V_{g1}) = 5.6\text{ nC}/15\text{ V} = 37\text{ nF} \)

(ii) \( C_n = 3\text{ nF} \)

An underestimate of the fall time results if figure 7.5a is used for both turn-on and turn-off calculations.\( C_n = 3.7\text{ nF} \) and \( t_f = 39\text{ ns} \).

### 7.2 Application of the Thyristor

The basic gate requirements to trigger a thyristor into the conduction state are that the current supplied to the gate is
- of adequate amplitude and sufficiently short rise time
- of sufficient duration.

The gate conditions are subject to the anode being forward-biased with respect to the cathode. Figure 7.6 illustrates a typical thyristor gate current waveform for turn-on.
either a positive or negative half sinusoidal cycle. The conduction angle, and therefore the speed of the 

If \( -V_{BO} \) and \( +V_{BO} \) are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half sinusoidal cycle. The conduction angle, and therefore the speed of the 

During each half cycle of the mains sinewave, \( C_2 \) charges until the voltage being applied to the diac reaches either of its breakover levels. The diac then conducts and \( C_2 \) discharges into the gate of the triac, switching it on. If \( -V_{BO} \) and \( +V_{BO} \) are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half sinusoidal cycle. The conduction angle, and therefore the speed of the 

A light dimmer circuit using a triac power control element, triggered via the diac, is shown in figure 7.8b. The potentiometer \( R_2 \) determines the phase difference between the ac mains sine wave and the voltage across \( C_2 \). This in turn sets the triac triggering angle, whence the lamp intensity.

The resistance of the diac is high as long as the voltage across it remains within its breakover voltage limits, \( \pm V_{BO} \). Each half cycle of the mains charges \( C_2 \) via \( R_1 \), \( R_2 \) and \( R_3 \) until the voltage being applied to the diac reaches either of its breakover levels. The diac then conducts and \( C_2 \) discharges into the gate of the triac, switching it on. If \( -V_{BO} \) and \( +V_{BO} \) are equal and opposite, the triac will be triggered at the same time after the start of either a positive or negative half sinusoidal cycle. The conduction angle, and therefore the speed of the 

Some form of filter is needed to comply with regulations concerning conducted and radiated interference. The simple LC filter shown within the dashed-lined box in figure 7.8b may be adequate. The values of the filter components will vary, but a combination of 0.15mF capacitor and a low Q inductor of 2.5mH is generally sufficient for the circuit to meet EMC limits. Circuits with intermittent loads, as with drills, sawing machines, and food mixers, are generally outwith EMC filtering regulations.

A motor speed control circuit, for electric drills, that employs back EMF to compensate for changes in motor load and mains voltage is shown in figure 7.9a. The series resistors \( R_1 \), \( R_2 \), \( R_3 \) and diode \( D_1 \) determine the phase difference between the ac mains sine wave and the voltage across \( C_2 \). The zinc oxide voltage dependent resistor, \( U \), minimises the possibility of damage to the triac due to high voltage transients that may be superimposed on the mains supply voltage.

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Stable Firing at Small Conduction Angles

The trigger network of the circuit shown in figure 7.9c has been modified by the addition of a capacitor C1 and diode D1. The diode clamps the capacitor potential at zero during the negative going half cycles of the mains input. The waveform developed across the capacitor has a positive slope to 140°, allowing thyristor triggering to be delayed to this point. As R2 is decreased, the peak of the waveform at the gate moves towards 90° as shown in figure 7.9d. As the speed increases, the no load firing angle also advances by a similar amount so stability will be maintained. This circuit will give smoother and more stable performance than the circuit of figure 7.9a. It will, however, give a marginally greater speed drop for a given motor loading at low speed settings. At the maximum speed settings the circuit of figure 7.9a approximates to that of figure 7.9c.

Improved Motor Performance with Stable Firing

The circuits in figure 7.9a and c have gate voltage waveforms that are of near linear slope from the zero point of each positive half cycle, as seen in figures 7.9b and d. This means that the only time that thyristor firing can be advanced in the mains cycle, say at 20°, is when the back EMF and hence motor speed is low. This effect tends to prevent smooth running at high speeds and high loads. Stable triggering, at low angles, can be achieved if the gate voltage ramp starts each cycle at a small positive level. This means that the time to reach the minimum trigger voltage is reduced. This is achieved by the circuit in figure 7.9e, where the capacitor C1 is charged during positive half cycles via resistor R1 and diode D1. During negative half cycles the only discharge path for C1 is via resistors R2 and R3. Diode D2 isolates the triggering circuit when the thyristor is ON. Resistor R4 adjusts minimum speed, and by effectively bleeding a constant current, in conjunction with the gate current from the triggering circuit, it enables resistor R2 to give consistent speed settings.

Circuit Design

If the speed controller is to be effective it must have stable thyristor firing angles at all speeds and give the best possible speed regulation with variations of motor load. The circuit in figure 7.9e gives a motor performance that satisfies both these requirements.

There are two factors that are important in the circuit operation in order to obtain the mentioned requirements:
- the value of positive slope of the waveform appearing at the thyristor gate.
- the phase angle at which the positive peak gate voltage is reached during a positive half cycle of ac mains input.

As described, the charging of capacitor C1 through resistor C1 determines the rate of rise of voltage at the thyristor gate during the positive half cycle. However, resistor R1 must also have a resistance such that several times the maximum thyristor gate current passes through D1. This current will then give consistent speed settings with the spread of thyristor gate currents when the minimum speed is set by resistor R4.

The positive slope value of the thyristor gate voltage is fixed according to the motor used. A motor that gives a smooth back EMF voltage will allow a low slope value to be used, giving good torque speed characteristics.

Some motors have coarser back EMF waveforms, with voltage undulations and spikes, and a steeper slope of thyristor gate voltage must be used in order to obtain stable motor operation. Capacitor C1 is chosen to provide the required positive slope of the thyristor gate voltage.

Analysis of the circuit of figure 7.9e allows the simplified form in figure 7.11a, where it is assumed that current flowing to the thyristor gate is small compared with the current flowing through resistor R1. An expression can be derived for the voltage that appears at the anode of D2 in terms of R1, R2 and C1. Specific component values give the thyristor gate waveforms shown in figure 7.11b.
In order to adjust the circuit to match a given motor, the back EMF of the motor must be known. This may be measured using the arrangement shown in figure 7.12. The voltage appearing across the motor is measured during the period when the series diode is not conducting (period A). The voltage so obtained will be the motor back EMF at its top speed on half wave operation, and corresponds to the back EMF that would be obtained from the unloaded motor at its highest speed when thyristor controlled. In practice, since the mains input is a sine wave, there is little increase in the 'no load' speed when the firing angle is reduced to less than about 70°.

The resistance $R_2$ in figure 7.9e determines the motor 'no load' speed setting. The waveforms of figure 7.11b may be used as a guide to obtaining the resistance value. It must be chosen so that at 70° and at its highest value, the gate voltage is higher than the measured back EMF by about 2V - the forward gate/cathode voltage of the thyristor. The thyristor is turned on when a trigger waveform, shown in figure 7.11b, exceeds the back EMF by the gate/cathode voltage. So, if the back EMF varies within a cycle then there will be a cycle to cycle variation in the firing angle. Normally, random variations of the firing angle by 20° are tolerable.

If, for example, there were variations in the back EMF of 1V, then with a firing angle of 70° and a capacitor of 32µF, the variation is about 12°. With capacitor values of 50µF and 64µF the firing angles are 19° and 25° respectively. Therefore, 50µF is suitable.

In order to make the gate voltage waveforms shown in figure 7.11b may be used as a guide to obtaining the resistance value. It must be chosen so that at 70° and at its highest value, the gate voltage is higher than the measured back EMF by about 2V - the forward gate/cathode voltage of the thyristor. The thyristor is turned on when a trigger waveform, shown in figure 7.11b, exceeds the back EMF by the gate/cathode voltage. So, if the back EMF varies within a cycle then there will be a cycle to cycle variation in the firing angle. Normally, random variations of the firing angle by 20° are tolerable.

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7.2.2 Thyristor gate drive design

In order to design a thyristor gate interface circuit, both the logic and thyristor gate requirements must be specified.

Consider interfacing a typical TTL-compatible microprocessor peripheral which offers the following specifications:

\[ I_{TT} = 0.3 \text{mA} \theta V_{OH} = 2.4\text{V} \]
\[ I_{LS} = 1.8 \text{mA} \theta V_{OL} = 0.4\text{V} \]
\[ V_{CC} = 5\text{V} \]

These specifications are inadequate for turning on a power thyristor or an optical interfacing device. If the power thyristor gate, worst case requirements are:

\[ I_{GT} = 75 \text{mA} \theta V_{GT} = 3 \text{V} \theta -65^\circ\text{C} \]

Then a power interfacing circuit is necessary. Figure 7.14 shows an interfacing circuit utilising a p-channel MOSFET with the following characteristics:

\[ C_{gs} = 400 \text{pF} \theta V_{th} = 3\text{.0V} \]
\[ R_{on} = 10 \text{ohms} \theta J_f = 0.5\text{A} \]

The resistor \( R_1 \) limits the MOSFET \( C_{gs} \) capacitance-charging current and also specifies the MOSFET turn-on time. If the charging current is to be limited to 1.8 mA when \( V_{OL} = 0.4 \text{V} \), then:

\[ R_1 = \frac{(V_{OH} - V_{LS})}{I_{OL}} \text{ (ohms)} \]
\[ = \frac{(5\text{V} - 0.4\text{V})}{1.8\text{mA}} = 2.7 \text{kilohms} \]

Figure 7.14. Interfacing a microprocessor to a power thyristor.

A smaller resistance could be used but this would not preserve the microprocessor low-voltage output level integrity if it were also being used as input to TTL logic. The MOSFET will not turn on until \( C_{gs} \) has charged to 3 V or, with a 5 V rail, approximately one \( R-C \) time constant. That is:

\[ t_{on} = RC_{gs} \text{ (s)} \]
\[ = 2.7 \text{kilohms} \times 400 \text{pF} = 1 \mu\text{s} \]

The MOSFET must provide the thyristor gate current and the current through resistor \( R_1 \) when the gate is at 3 V.

The maximum value of resistor \( R_2 \) is when \( R_2 = \infty \) and is given by:

\[ R_2 = \frac{V_{CC} - I_{GT}R_1}{I_{GT} + R_1} \]
\[ = \frac{5\text{V} - 3\text{V} - 75 \text{mA} \times 100\text{ohms}}{75 \text{mA}} = 16.6 \text{ohms} \]

Use \( R_2 = 10 \text{ohms} \).

The resistor \( R_3 \) provides a low cathode-to-cathode impedance in the off-state, thus improving SCR noise immunity. When \( V_{OL} = 3 \text{V} \),

\[ I_{OL} = \frac{V_{OL} - V_{GT}}{R_{on} + R_1} = \frac{5\text{V} - 3\text{V}}{100\text{ohms}} = 100 \text{mA} \]

7.3 Drive design for GCT and GTO thyristors

The gate turn-off thyristor is not only turned on from the gate but, as its name implies, is turned off from its gate with negative gate current. Basic GTO thyristor gate current requirements are similar to those for the power bipolar transistor (now virtually obsolete) when reverse base current is used for BJT turn-off.
Figure 7.16 shows a gate drive circuit for a GTO thyristor which is similar to that historically used for power bipolar junction transistor base drives. The inductor $L$, in figure 7.16, is the key turn-off component since it controls the $di/dt$ of the reverse gate current. The smaller the value of $L$, the larger the reverse $di/dt$ and the shorter the turn-off time. But with a shorter turn-off time the turn-off gain decreases, eventually to unity. That is, if the GTO thyristor is switched off rapidly, the reverse gate current must be of the same magnitude as the anode current to be extinguished. A slowly applied reverse gate current $di/dt$ can produce a turn-off gain of over 20 but at the expense of increased turn-off saturation delay and switching losses. For the GTO thyristor $L$ is finite to get a turn-off gain of more than one, while to achieve unity gain turn-off for the GCT, $L$ (which includes stray inductance) is minimised.

The GTO thyristor cathode-to-gate breakdown voltage rating $V_{bsw}$ specifies the maximum negative rail voltage. A level of -15 to -20V is common, and for supply rail simplicity a ±15 V rail may be selected. Resistor $R_2$ limits the base current of $T_t$. If an open collector TTL driver is employed, the current through $R_4$ is given by

$$I_{on} = (V_{cc} - V_{be}) / R_4$$ (A)

For the open collector 74 ttl series, $I_{on} = 40 \text{mA}$ when $V_{cc} = 0.5 \text{V}$ whence $R_2$ can be specified. The resistor $R_2$ speeds up turn-off of $T_t$. It is as large as possible to ensure that minimal base current is diverted from $T_t$. Diodes $D_o$ and $D_a$ form a Baker’s clamp, preventing $T_t$ from saturating thereby minimising its turn-off delay time.

![Figure 7.16. Gate drive circuit and anode snubber circuits for a GTO thyristor.](image)

The two driver transistors $T_n$ and $T_p$ should

- have high gains,
- be fast switching,
- have collector voltage ratings in excess of $V_{cc} + V_{ex}$.

The GTO thyristor gate turn-on current is determined by resistor $R_{sw}$, which is specified by

$$R_{sw} = (V_{cc} - V_{be} - V_{ex}) / I_{sw}$$ (Ohms)

The power rating of $R_{sw}$ is given by

$$P_{sw} = (V_{cc} - V_{be} - V_{ex})I_{sw}$$ (W)

where $\delta$ is the maximum on-state duty cycle. The capacitor $C_{sw}$ in parallel with $R_{sw}$ provides a short current boost at turn-on, as shown in figure 7.6, thereby speeding up thyristor turn-on, increasing turn-on $di/dt$ capability, and reducing turn-on losses.

The series resistors $R_1$ and $R_2$ bias the bases of the totem pole level shift driver and, for an on-condition, the potential of point $X$ in figure 7.16 is given by

$$V_X = V_{be} + V_{ex}$$ (V)

The total current flow through $R_1$ is made up of the transistor $T_n$ base current and that current flowing through $R_2$, that is

$$I_{sw} = I_{be} + V_{be} / R_1$$ (A)

from which

$$R_1 = (V_{be} - V_{be}) / I_{be}$$ (ohms)

The power rating of $R_1$ is

$$P_1 = (V_{be} - V_{be}) I_{be}$$ (W)

For fast turn-off, if the reverse gate current at turn-off is to be of the same magnitude as the maximum anode current, then $R_2$ must allow sufficient base current to drive $T_n$. That is

$$R_2 = (V_{be} + V_{ex}) / I_{be}$$ (ohms)

Once the gate-to-cathode junction of the GTO has recovered, the reverse gate current decays to the leakage level. The power rating of $R_2$ can be low at lower switching frequencies. The small inductor $L$ in the turn-off circuit is of the order of microhenrys and it limits the rate of rise of reverse gate current, while $R_4$ damps any inductor current oscillation. The turn-on and turn-off BJT output totem pole in figure 7.16 can be replaced by suitable n-channel MOSFET circuitry in high power GCT and GTO thyristor applications. In high power IGBT applications, MOSFETs and rail decoupling electrolytic capacitors are extensively parallel connected. Typically 21 capacitors and 42 MOSFETs are parallel connected to provide a low impedance path for unity anode current extraction from the GCT gate. The gate inductance (including the GCT internal package inductance) is minimised, whence $L$ is zero. Typically, the IGBT gate drive, gate connection, and internal package inductance are each about 2nH. This is achieved by minimising lengths, capacitive decoupling, and using parallel go and return paths. As a result, gate reverse $di/dt$s of over 5kA/µs are attainable with a ~15V dc negative gate supply.

**Table 7.4: Gate drive isolation techniques summary**

<table>
<thead>
<tr>
<th>Technique</th>
<th>data transfer</th>
<th>power transfer</th>
<th>comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transformer</td>
<td>direct signal coupling</td>
<td>direct magnetic transfer</td>
<td>duty cycle limited</td>
</tr>
<tr>
<td>opto-coupler</td>
<td>slow, with capacitive effects</td>
<td>n/a</td>
<td>voltage and dvdt limit</td>
</tr>
<tr>
<td>fibre optics</td>
<td>fast, virtually no voltage limit</td>
<td>n/a</td>
<td>best signal transmission at MV and HV</td>
</tr>
<tr>
<td>charge couple</td>
<td>n/a</td>
<td>requires switching</td>
<td>induced effects between ground level and gate level, LV application</td>
</tr>
<tr>
<td>bootstrap</td>
<td>n/a</td>
<td>requires switching</td>
<td>induced effects between ground level and gate level, LV application</td>
</tr>
</tbody>
</table>
Problems

7.1. Calculate suitable resistor values for the triac gate drive circuit in figure 7.7a, assuming a minimum gate current requirement of 50 mA and the gain of Q1 is 50 at 50 mA.

7.2. Repeat problem 7.1 for the circuits in figures
   • 7.7b
   • 7.7c
   • 7.7d.

7.3. Repeat example 7.2 assuming a 2V triac gate threshold voltage for turn-on.