CHAPTER 17

DC to AC Inverters – Switched Mode

Inversion is the conversion of dc power to ac power at a desired output voltage or current and frequency. A static semiconductor inverter circuit performs this electrical energy inverting transformation. The terms voltage-fed and current-fed are used in connection with the output from inverter circuits.
A *voltage-source inverter* (VSI) is one in which the dc input voltage is essentially constant and independent of the load current drawn. The inverter specifies the load voltage while the drawn current shape is dictated by the load. Being a voltage source, an open circuit output is allowable.
A *current-source inverter* (CSI) is one in which the source, hence the load current is predetermined and the load impedance determines the output voltage. The supply current cannot change quickly. This current is controlled by series dc supply inductance which prevents sudden changes in current. The load current magnitude is controlled by varying the input dc voltage to the large inductance, hence inverter response to load changes is slow. Being a current source, the inverter can survive an output short circuit thereby offering fault ride-through properties, but an open circuit output is problematic.
In the case of a VSI, voltage control may be required to maintain a fixed output voltage when the dc input voltage regulation is poor, or to control load power. The inverter output can be single-phase, three-phase or multi-phase. Variable output frequency may be required for ac motor speed control where, in conjunction with voltage or current control, constant (controlled) motor flux can be maintained.
Inverter output waveforms (either voltage or current) are usually rectilinear in nature and as such contain harmonics which may lead to reduced load efficiency and performance. Load harmonic reduction can be achieved by either filtering, selected harmonic-reduction chopping or pulse-width modulation.

The quality of an inverter output is normally evaluated in terms of its *harmonic factor*, ρ, *distortion factor*, μ, and *total harmonic distortion*, *thd*. In section 15.7.2 these first two factors were defined in terms of the supply current. For VSI inverters the factors are redefined in terms of the output voltage harmonics as follows

$$\rho_n = \left|\frac{V_n}{V_1}\right| = n\mu_n \qquad n > 1 \tag{17.1}$$

The distortion factor for an individual harmonic is

$$\mu_n = \left|\frac{V_n}{nV_1}\right| = \frac{\rho_n}{n} \tag{17.2}$$

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]} \Big/ V_1 = \sqrt{\sum_{n\geq 2}^{\infty}\mu_n^2} = \sqrt{\sum_{n\geq 2}^{\infty}\left(\frac{\rho_n}{n}\right)^2} \tag{17.3}$$

The factor V_n/n is used since the harmonic currents produced in an inductive load attenuate with frequency. The harmonic currents produce unwanted heating and torque oscillations in ac motors, although such harmonic currents are not a drawback to the power delivered to a resistive heating load or an incandescent lighting load. Harmonics reflected back into the input may be problematic.

17.1 DC-to-ac voltage-source inverter bridge topologies

17.1.1 Single-phase voltage-source inverter bridge

Figure 17.1a shows an H-bridge inverter (VSI) for producing an ac voltage and employing switches which may be transistors (MOSFET or IGBT), or at high powers, thyristors (GTO or GCT). Device

conduction patterns are also shown in figures 17.1b and c. With inductive loads (not purely resistive), stored energy at turn-off is fed through the bridge reactive feedback or freewheel diodes D_1 to D_4. These four diodes clamp the load voltage to within the dc supply voltage rails (0 to V_s).

17.1.1i - *Square-wave (bipolar) output*
Figure 17.1b shows waveforms for a square-wave output ($2t_1 = t_2$) where each device is turned on as appropriate for 180°, (that is π) of the output voltage cycle (state sequence 10, 01, 10, ..).
The load current i_L grows exponentially through T_1 and T_2 (state 10) according to

$$V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{17.4}$$

When T_1 and T_2 are turned off, T_3 and T_4 are turned on (state 01), thereby reversing the load voltage polarity. Because of the inductive nature of the load, the load current cannot reverse instantaneously and load reactive energy flows back into the supply via diodes D_3 and D_4 (which are in parallel with T_3 and T_4 respectively) according to

$$-V_s = L\frac{di_L}{dt} + i_L R \qquad \text{(V)} \tag{17.5}$$

The load current falls exponentially and at zero, T_3 and T_4 become forward-biased and conduct load current, thereby feeding power to the load.

The output voltage is a square wave of magnitude ± V_s, figure 17.1b, and has an rms value of V_s.
For a simple *R-L* load, with time constant $\tau = L/R$, during the first cycle with no initial load current, solving equation (17.4) yields a load current

$$i_L(t) = \frac{V_s}{R}\left(1 - e^{\frac{-t}{\tau}}\right) \qquad \text{(A)} \tag{17.6}$$

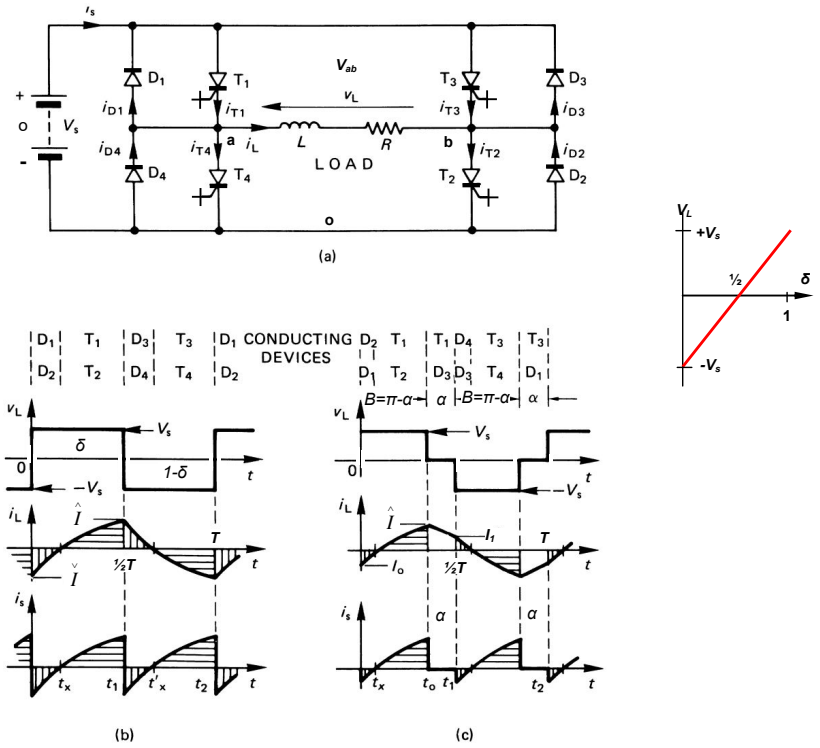


Figure 17.1. *GCT thyristor single-phase bridge inverter:*
(a) circuit diagram; (b) square-wave output voltage; and (c) quasi-square-wave output voltage.

Under steady-state load conditions, the initial current is $\check{I}$ as shown in figure 17.1b, and equation (17.4) yields

$$i_L(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - \check{I}\right)e^{\frac{-t}{\tau}} \quad \text{(A)} \qquad 0 \le t \le t_1 = \tfrac{1}{2}T \quad \text{(s)} \tag{17.7}$$

for $v_L = V_s$ (V)

$\check{I} \le 0$ (A)

During the second half-cycle ($t_1 \le t \le t_2$) when the supply is effectively reversed across the load, equation (17.5) yields

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + \hat{I}\right)e^{\frac{-t}{\tau}} = -\frac{V_s}{R}\left(1 - \left(1 + \tanh\left(\frac{t_1}{2\tau}\right)\right)e^{\frac{-t}{\tau}}\right) \quad \text{(A)} \qquad 0 \le t \le t_2 - t_1 = \tfrac{1}{2}T \quad \text{(s)} \tag{17.8}$$

for $v_L = -V_s$ (V)

$\hat{I} \ge 0$ (A)

A new time axis has been used in equation (17.8) starting at $t = t_1$ in figure 17.1b. Since in steady-state by symmetry, $\hat{I} = -\check{I}$, the initial steady-state current $\hat{I}$ can be found from equation (17.7) when, at $t = t_1$, $i_L = \hat{I}$ yielding

$$\hat{I} = -\check{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_1}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}} = \frac{V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right) \quad \text{(A)} \tag{17.9}$$

The zero current cross-over point t_x, shown on figure 17.1b, can be found by solving equation (17.7) for $t = t_x$ when $i_L = 0$, which yields

$$t_x = \tau\,\ell n\left(1 - \frac{\check{I}R}{V_s}\right) = \tau\,\ell n\left(1 + \frac{\hat{I}R}{V_s}\right) \quad \text{(s)} \tag{17.10}$$

The average thyristor current, $\bar{I}_T$, average diode current, $\bar{I}_D$, and mean source current, $\bar{I}_s$ can be found by integration of the load current over the appropriated bounds shown in the following integrals.

$$\bar{I}_T = \frac{1}{t_2}\int_{t_x}^{t_1} i_L(t)\,dt = \frac{1}{t_2}\left[\frac{V_s}{R}(t_1 - t_o) + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - e^{\frac{-t_o}{\tau}}\right)\right] \tag{17.11}$$

where i_L is given by equation (17.7) and

$$\bar{I}_D = \frac{1}{t_2}\int_0^{t_x} -i_L(t)\,dt = \frac{1}{t_2}\left[-\frac{V_s}{R}t_x - \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_x}{\tau}} - 1\right)\right] \tag{17.12}$$

where i_L is given by equation (17.8).

Inspection of the source current waveform in figure 17.1b shows that the average dc voltage source current is related to the average semiconductor device currents by

$$\bar{I}_s = 2\left(\bar{I}_T - \bar{I}_D\right) = \frac{1}{t_2}\left[\frac{V_s}{R}t_1 + \tau\left(\frac{V_s}{R} + \hat{I}\right)\left(e^{\frac{-t_1}{\tau}} - 1\right)\right] \tag{17.13}$$

The steady-state mean power delivered by the dc supply and absorbed by the resistive load component R is given by

$$P_L = \frac{1}{t_1}\int_0^{t_1} V_s\, i_L(t)\;dt \;=\; V_s\bar{I}_s \quad \left(= I_{Lrms}^2 R\right) \quad \text{(W)} \tag{17.14}$$

where $i_L(t)$ is given by equation (17.7). Rather than integration involving equations (17.7) and (17.8), the mean load power can be used to determine the rms load current:

$$i_{Lrms} = \sqrt{P_L/R} = \sqrt{V_s\bar{I}_s/R} \quad \text{(A)} \tag{17.15}$$

The rms output voltage is V_s and the output fundamental frequency f_o is $f_o = 1/T = 1/2t_1 = 1/t_2$.

The instantaneous output voltage expressed as a Fourier series is given by

$$V_L = \frac{4}{\pi}V_s\sum_{n\,odd}^{\infty}\frac{1}{n}\sin n\omega_o t \quad \text{(V)} \tag{17.16}$$

where $\omega_o = 2\pi f_o = 2\pi / t_2 = 2\pi / T$ and for n = 1 the magnitude of the fundament frequency f_o is $4/\pi V_s$ which is an output rms fundamental voltage v_{o1} of

$$v_{o1} = \frac{2\sqrt{2}}{\pi}V_s = 0.90V_s \quad \text{(V)} \tag{17.17}$$

The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$i_L(\omega t) = \frac{4}{\pi}V_s\sum_{n=1,3,5}^{\infty}\frac{1}{nZ_n}\sin\left(n\omega_o t - \phi_n\right) = \sum_{n=1,3,5}^{\infty} I_n\sin\left(n\omega_o t - \phi_n\right) \tag{17.18}$$

where $I_n = \frac{4}{\pi}\frac{V_s}{nZ_n}$ whence $I_{n\text{rms}} = \frac{I_n}{\sqrt{2}}$

$Z_n = \sqrt{R^2 + (n\omega_o L)^2}$ $\qquad \phi_n = \tan^{-1} n\omega_o L/R$ $\qquad$ such that $\cos\phi_1 = R/Z_1$

The fundamental output power is

$$P_1 = I_1^2 R = \left(\frac{v_{o1}}{Z_1}\right)^2 R = \frac{V_s^2}{R}\left(\frac{2\sqrt{2}}{\pi}\right)^2\cos^2\phi_1 \tag{17.19}$$

The load power is given by the sum of each harmonic i^2R power component, that is

$$P_L = \sum_{n=1,3,5}^{\infty}\left(I_n/\sqrt{2}\right)^2 R = \sum_{n=1,3,5}^{\infty} I_{n\,rms}^2 R \quad \left(= V_s\bar{I}_s\right) \tag{17.20}$$

Alternately, after integrating equation (17.14), with the load current from equation (17.8)

$$P_L = \frac{V_s^2}{R}\left(1 - \frac{2\tau}{t_1}\frac{1 - e^{\frac{-t_1}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}}\right) = \frac{V_s^2}{R}\left(1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)\right) \tag{17.21}$$

From $P_L = i_{rms}^2 R$ the rms loads current is

$$i_{Lrms} = \frac{V_s}{R}\sqrt{1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)} \tag{17.22}$$

The load power factor is given by

$$pf = \frac{P}{S} = \frac{i_{Lrms}^2 R}{i_{Lrms}v_{rms}} = \sqrt{1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)} \tag{17.23}$$

17.1.1ii - *Quasi-square-wave (multilevel) output*

The rms output voltage form an H-bridge can be varied by producing a quasi-square output voltage ($2t_1 = t_2$, $t_0 < t_1$) as shown in figure 17.1c. After T_1 and T_2 have been turned on (state 10), at the angle α one device is turned off. (One leg is phase shifted α relative to the other leg.) If T_1 is turned off (and T_4 is turned on after a short delay), the load current slowly freewheels through T_2 and D_4 (state 00) in a zero voltage loop according to

$$0 = L\frac{di_L}{dt} + i_L R \quad \text{(V)} \tag{17.24}$$

When T_2 is turned off and T_3 turned on (state 01), the remaining load current rapidly reduces to zero back into the dc supply V_s, through diodes D_3 and D_4. When the load current reaches zero, T_3 and T_4 become forward biased and the output current reverses, through T_3 and T_4.

The output voltage shown in figure 17.1c consists of a sequence of non-zero voltages $\pm V_s$, alternated with zero output voltage periods. During the zero output voltage period a diode and switch conduct, firstly T_1 and D_3 in the first period, and T_3 and D_1 in the second zero output period. In each case, a *zero voltage loop* is formed by a switch, diode, and the load. The next two zero output sequences would be T_2 and D_4 then T_4 and D_2, forming *alternating zero voltage loops* (sequence 10, 00, 01, 11, 10, ..) rather than repeating a continuous T_1 and D_3 then T_3 and D_1 sequence of zero voltage loops (sequence 10, 11,

01, 11, 10, .. or sequence 10, 00, 01, 00, 10, ..). By alternating the zero voltage loops (between states 00 and 11), losses are uniformly distributed between the semiconductors, device switching frequency is half that experienced by the load, and a finer output voltage resolution is achievable.
With reference to figure 17.1c, the load current i_L for an applied quasi square-wave voltage is defined as follows.

(i) $v_L > 0$

$$i_{L_I}(t) = \frac{V_s}{R} - \left(\frac{V_s}{R} - I_o\right)e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_o \qquad (17.25)$$

for $I_o \le 0$ (A)

(ii) $v_L = 0$

$$i_{L_{II}}(t) = \hat{I}\, e^{\frac{-t}{\tau}} \qquad 0 \le t \le t_1 - t_o \qquad (17.26)$$

for $\hat{I} \ge 0$ (A)

(iii) $v_L < 0$

$$i_L(t) = -\frac{V_s}{R} + \left(\frac{V_s}{R} + I_1\right)e^{\frac{-t}{\tau}} = -i_{L_I}(t) \qquad 0 \le t \le t_o \qquad (17.27)$$

for $I_1 \ge 0$ (A)

The currents I_o, $\hat{I}$, and I_1 are given by

$$I_o = -\frac{V_s}{R}\,\frac{e^{\frac{-t_1+t_o}{\tau}} - e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \quad \text{(A)} \qquad (17.28)$$

$$\hat{I} = \frac{V_s}{R}\,\frac{1-e^{\frac{-t_o}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} \quad \text{(A)} \qquad (17.29)$$

$$I_1 = -I_o \quad \text{(A)} \qquad (17.30)$$

The zero current cross-over instant, t_x, shown in figure 17.1c, is found by solving equation (17.25) for t when i_L equals zero current.

$$t_x = \tau\,\ell n\left(1 - \frac{I_o R}{V_s}\right) = \tau\,\ell n\left(1 + \frac{I_1 R}{V_s}\right) \qquad (17.31)$$

The average thyristor current, $\bar{I}_T$, average diode current, $\bar{I}_D$, and mean source current, $\bar{I}_s$ can be found by integration of the load current over the shown bounds (assuming alternating zero volt loops).

$$\bar{I}_T = \frac{1}{t_2}\int_{t_x}^{t_1} i_{L_I}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i_{L_{II}}(t)\,dt \qquad (17.32)$$

where i_L is given by equations (17.25) and (17.26) for the respective integrals, and

$$\bar{I}_D = \frac{1}{t_2}\int_0^{t_x} -i_{L_I}(t)\,dt + \frac{1}{2t_2}\int_0^{t_1-t_o} i_{L_{II}}(t)\,dt \qquad (17.33)$$

where i_L is given by equations (17.25) and (17.26) for the respective integrals.

Inspection of the source current waveform in figure 17.1c shows that the average source current is related to the average semiconductor device currents by

$$\bar{I}_s = \frac{1}{t_1}\int_0^{to} i_{L_I}(t)dt = 2\left(\bar{I}_T - \bar{I}_D\right) \qquad (17.34)$$

The steady-state mean load and dc source powers are

$$P_L = \frac{1}{t_1}\int_0^{t_o} V_s\, i_L(t)\;dt \;=\; V_s\bar{I}_s \qquad \left(= I^2_{Lrms}R\right) \qquad \text{(W)} \qquad (17.35)$$

where $i_L(t)$ is given by equation (17.25). The mean load power can be used to determine the rms load current:

$$I_{Lrms} = \sqrt{P_L/R} = \sqrt{V_s\bar{I}_s/R} \qquad \text{(A)} \qquad (17.36)$$

The output fundamental frequency f_o is $f_o = 1/2t_1 = 1/t_2$.

The variable rms output voltage, for $0 \le \alpha \le \pi$, is

$$v_{rms} = \sqrt{\frac{1}{t_1}\int_0^{t_o} V_s^2 dt} = \sqrt{1-\alpha/\pi}\;V_s \qquad (17.37)$$

and the output fundamental frequency f_o is $f_o = 1/t_2$. This equation for rms output voltage shows that only the n^{th} harmonic can be eliminated when $\cos ½n\alpha = 0$, that is for $\alpha = \pi/n$. In so eliminating the n^{th} harmonic, from equation (17.38), the magnitude of the fundamental is reduced to $4/\pi V_s \cos\alpha/n$.
The output voltage V_L in its Fourier coefficient series form is given by

$$V_L = \frac{4}{\pi}V_s \sum_{n\,odd}^{\infty} \frac{\cos ½n\alpha}{n}\sin n\omega_o t \qquad \text{(V)} \qquad (17.38)$$

and for n = 1, the rms fundamental of the output voltage v_{o1} is given by

$$v_{o1} = \frac{2\sqrt{2}}{\pi}V_s \cos ½\alpha = 0.90 \times V_s \times \cos ½\alpha \qquad \text{(V)} \qquad (17.39)$$

The characteristics of these load voltage harmonics are shown in figure 17.2.

An alternative approach is to consider the control of one leg phase shifted by β radians with respect of the other leg. The phase output voltage for each leg, with respect to the supply (artificial) mid point, o, is

$$V_{ao} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi}\sin n\omega_o t$$

$$V_{bo} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi}\sin\left(n\left(\omega_o t - \beta\right)\right)$$

The output V_{ab} is then given by the difference, that is

$$V_{ao} - V_{bo} = V_{ab} = \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi}\sin n\omega_o t - \sum_{n=1,3,5,\ldots}^{\infty} \frac{2V_s}{n\pi}\sin\left(n\left(\omega_o t - \beta\right)\right)$$

$$= \sum_{n=1,3,5,\ldots}^{\infty} \frac{4V_s}{n\pi}\sin ½n\beta\cos n\omega_o t$$

Expressing the phase shift angle β in terms of the delay angle α, where $\beta = \pi - \alpha$, yields equation (17.38).

The load current can be expressed in terms of the Fourier voltage waveform series, that is

$$i_L(\omega t) = \frac{V_L}{Z_L} = \frac{4}{\pi}V_s \sum_{n=1,3,..}^{\infty} \frac{\cos ½n\alpha}{nZ_n}\sin\left(n\omega_o t - \phi_n\right) = \sum_{n=1,3,5,..}^{\infty} I_n \sin\left(n\omega_o t - \phi_n\right) \qquad (17.40)$$

where $I_n = \frac{4}{\pi}\frac{V_s}{nZ_n}\cos ½n\alpha$ whence $I_{n\,\text{rms}} = \frac{I_n}{\sqrt{2}}$

$$Z_n = \sqrt{R^2 + (n\omega_o L)^2} \qquad \phi_n = \tan^{-1} n\omega_o L/R$$

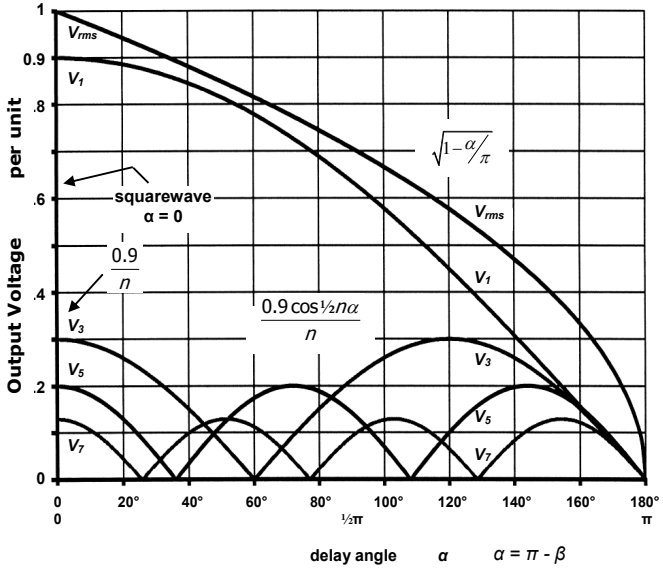


Figure 17.2. *Full bridge inverter output voltage harmonics normalised with respect to square wave rms output voltage, V_{rms}=V_s.*

The load power is given by the sum of each harmonic i^2R power component, that is

$$P_L = \sum_{n=1,3,5}^{\infty} \left(I_n/\sqrt{2}\right)^2 R = \sum_{n=1,3,5,\ldots}^{\infty} I_{n\,rms}^2 R \qquad \left(= V_s \bar{I}_s\right) \tag{17.41}$$

The load power and rms current can be evaluated from equations (17.21) and (17.22) provided the rms voltage given by equation (17.37) replaces V_s. That is

$$P_L = \frac{V_s^2}{R}\left(1 - \alpha/\pi\right)\left(1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)\right) = i_{Lrms}^2 R \tag{17.42}$$

$$i_{Lrms} = \frac{V_s}{R}\sqrt{1 - \alpha/\pi}\sqrt{1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)} \tag{17.43}$$

The load power factor is independent of α and is given by equation (17.23), that is

$$pf = \frac{P}{S} = \frac{i_{Lrms}^2 R}{i_{Lrms} v_{rms}} = \sqrt{1 - \frac{2\tau}{t_1}\tanh\left(\frac{t_1}{2\tau}\right)} \tag{17.44}$$

A variation of the basic four-switch dc to ac single-phase H-bridge is the half-bridge version where two series switches (one pole or leg) and diodes are replaced by a split two-capacitor voltage source, as shown in figure 17.3. This reduces the number of semiconductors and gate circuit requirements, but at the expense of halving the maximum output voltage. Example 17.3 illustrates the half-bridge and its essential features. Behaviour characteristics are as for the full-bridge, square-wave, single-phase inverter but V_s is replaced by ½V_s in the appropriate equations. Only a rectangular-wave bipolar output voltage can be obtained. Since zero volt loops cannot be created, no rms voltage control is possible. The rms output voltage is ½V_s, while the output power is a quarter that of the full H-bridge.

Example 17.1: ***Single-phase H-bridge with an L-R load***

A single-phase H-bridge inverter, as shown in figure 17.1a, supplies a 10 Ω resistance with inductance 50 mH, from a 340 V dc source. If the bridge is operating at 50 Hz (output), determine the average supply current and the load rms voltage and current and steady-state current waveforms with

i. a square-wave output
ii. a symmetrical quasi-square-wave output with a 50 per cent on-time.

Solution

The time constant of the load, τ = 0.05mH/10Ω = 5 ms, t_1 = 10ms and t_2 = 20ms.

i. The output voltage rms value is 340 V ac.
Equation (17.9) gives the load current at the time when the supply polarity is reversed across the load, as shown in figure 17.1b, that is

$$\hat{I} = -\check{I} = \frac{V_s}{R}\frac{1 - e^{\frac{-t_2}{\tau}}}{1 + e^{\frac{-t_1}{\tau}}} \qquad \text{(A)}$$

where t_1 = 10 ms. Therefore

$$\hat{I} = -\check{I} = \frac{340\text{V}}{10\Omega} \times \frac{1 - e^{-2}}{1 + e^{-2}} \qquad \text{(A)}$$
$$= 25.9\text{A}$$

When v_L = +340 V, from equation (17.7) the load current is given by

$$i_L = 34 - (34 + 25.9) \times e^{-200t} = 34 - 59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

From equation (17.10) the zero current cross-over time, t_x, occurs $5\text{ms} \times \ell n(1 + 25.9\text{A} \times 10\Omega/340\text{V})$ = 2.83ms after load voltage reversal.
When v_L = -340 V, from equation (17.8) the load current is given by

$$i_L = -34 + (34 + 25.9) \times e^{-200t} = -34 + 59.9e^{-200t} \qquad 0 \le t \le 10 \text{ ms}$$

The mean power delivered to the load is given by equation (17.14), that is

$$P_L = \frac{1}{10\text{ms}} \int_0^{10\text{ms}} 340\text{V} \times \{34 - 59.9 \times e^{-200t}\}\, dt$$
$$= 2755 \text{ W}$$

From $P = i^2R$, the load rms current is

$$i_{Lrms} = \sqrt{P_L/R} = \sqrt{2755\text{W}/10\Omega} = 16.60\text{A} \quad \text{and} \quad \bar{I}_s = P_L/V_s = 2755\text{W}/340\text{V} = 8.1\text{A}$$

These power and rms current results can be confirmed with equations (17.21) and (17.22).

ii. The quasi-square output voltage has a 5 ms on-time, t_o, and a 5 ms period of zero volts.
From equation (17.37) the rms output voltage is

$$V_s\sqrt{1 - 5\text{ms}/10\text{ms}} = V_s/\sqrt{2} = 240\text{V rms}.$$

The current during the different intervals is specified by equations (17.25) to (17.30). Alternately, the steady-state load current equations can be specified by determining the load current equations for the first few cycles at start-up until steady-state conditions are attained.

First 5 ms on-period when v_L = 340 V and initially i_L = 0 A

$$i_L = 34 - 34\, e^{-200t}$$

and at 5ms, i_L = 21.5A
First 5 ms zero-period when v_L = 0 V

$$i_L = 21.5\, e^{-200t}$$

and at 5ms, i_L =7.9A
Second 5 ms on-period when v_L = -340 V

$$i_L = -34 + (34+7.9) \times e^{-200t}$$

with i_L = 0 at 1 ms and ending with i_L = -18.6 A
Second 5 ms zero-period when v_L = 0 V

$$i_L = -18.6\, e^{-200t}$$

ending with i_L = -6.8A
Third 5 ms on-period when v_L = 340 V

$$i_L = 34 - (34+6.8) \times e^{-200t}$$

with i_L = 0 at 0.9 ms and ending with i_L = 19.0 A
Third 5 ms zero-period when v_L = 0 V

$$i_L = 19.0\, e^{-200t}$$

ending with i_L = 7.0A
Fourth 5 ms on-period when v_L = -340 V

$$i_L = -34 + (34+7.0) \times e^{-200t}$$

with i_L = 0 at 0.93 ms and ending with i_L = -18.9 A
Fourth 5 ms zero-period when v_L = 0 V

$$i_L = -18.9\, e^{-200t}$$

ending with i_L = -7.0A

Steady-state load current conditions have been reached and the load current waveform is as shown in figure 17.1c. Convergence of an iterative solution is more rapid if the periods considered are much longer than the load time constant (and vice versa).
The mean load power for the quasi-square wave is given by

$$P_L = \frac{1}{10\text{ms}} \int_0^{5\text{ms}} 340\text{V} \times \{34 - 41 \times e^{-200t}\}\, dt$$
$$= 1378 \text{ W}$$

The load rms and supply currents are

$$i_{Lrms} = \sqrt{P_L/R} = \sqrt{1378\text{W}/10\Omega} = 11.74\text{A} \qquad \bar{I}_s = P_L/V_s = 1378\text{W}/340\text{V} = 4.05\text{A}$$

♣

Example 17.2: ***H-bridge inverter ac output factors***

In each waveform case (square and quasi-square) of example 17.1a calculate

i. the average and peak current in the switches
ii. the average and peak current in the diodes
iii. the peak blocking voltage of each semiconductor type
iv. the average source current
v. the harmonic factor and distortion factor of the lowest order harmonic
vi. the total harmonic distortion

Solution

Square-wave

i. The peak current in the switch is $\hat{I}$ = 25.9 A and the current zero cross-over occurs at t_x =2.83ms. The average switch current, from equation (17.11) is

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{2.83\text{ms}}^{10\text{ms}} (34 - 59.9\, e^{-200t})\, dt$$
$$= 5.71 \text{ A}$$

ii. The peak diode current is 25.9 A. The average diode current from equation (17.12) is

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_{0}^{2.83\text{ms}} (34 - 59.9\, e^{-200t})\, dt$$
$$= 1.66 \text{ A}$$

iii. The maximum blocking voltage of each device is 340 V dc.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_T - \bar{I}_D\right) = 2\times(5.71\text{A} - 1.66\text{A}) = 8.10\text{A}$$

This results in the supply delivery power of 340Vdc × 8.10A = 2754W

v. From equation (17.16), with the third as the lowest harmonic, the distortion factors are

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \tfrac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{3V_1}\right| = \tfrac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi. From equation (17.16)

$$thd = \sqrt{\sum\left(\frac{V_n}{n}\right)^2}\Big/ V_1$$
$$= \sqrt{\left(\tfrac{1}{3}\right)^2 + \left(\tfrac{1}{5}\right)^2 + \left(\tfrac{1}{7}\right)^2 + \ldots\ldots}$$
$$= 46.2 \text{ per cent}$$

Quasi-square-wave, α = ½π (5 ms) and from equation (17.31) t_x = 0.93ms

i. The peak switch current is 18.9 A.
From equation (17.32) the average switch current, using alternating zero volt loops, is

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{0.93\text{ms}}^{5\text{ms}} (34 - 41e^{-200t})\, dt + \frac{1}{40\text{ms}}\int_{0}^{5\text{ms}} 19e^{-200t} dt$$
$$= 2.18 + 1.50 = 3.68 \text{ A}$$

ii. The peak diode current (and peak switch current) is 18.9 A. The average diode current, from equation (17.33), when using alternating zero volt loops, is given by

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_{0}^{0.93\text{ms}} \left(-34 + 41e^{-200t}\right) dt + \frac{1}{40\text{ms}}\int_{0}^{5\text{ms}} 19e^{-200t} dt$$
$$= 0.16 + 1.50 = 1.66 \text{ A}$$

iii. The maximum blocking voltage of each device type is 340 V.

iv. The average supply current is

$$\bar{I}_s = 2\left(\bar{I}_T - \bar{I}_D\right) = 2\times(3.68\text{A} - 1.66\text{A}) = 4.04\text{A}$$

This results in the supply delivery power of 340Vdc × 4.04A = 1374W

v. The harmonics are given by equations (17.1) to (17.3)

$$hf = \rho_3 = \left|\frac{V_3}{V_1}\right| = \tfrac{1}{3\sqrt{2}} \Big/ \tfrac{1}{\sqrt{2}} = \tfrac{1}{3}, \text{ that is, } 33\tfrac{1}{3} \text{ per cent}$$

$$df = \mu_3 = \left|\frac{V_3}{nV_1}\right| = \rho_3 / n = \tfrac{1}{9}, \text{ that is, } 11.11 \text{ per cent}$$

vi.

$$thd = \sqrt{\left[\sum_{n\geq 2}^{\infty}\left(\frac{V_n}{n}\right)^2\right]}\Big/ V_1$$
$$= \sqrt{\left(\frac{1}{3}\right)^2 + \left(\frac{-1}{5}\right)^2 + \left(\frac{1}{7}\right)^2 + \left(\frac{1}{9}\right)^2 + \ldots} \qquad = 46.2 \text{ per cent}$$

♣

Example 17.3: ***Harmonic analysis of H-bridge inverter with an L-R load***

For each delay case (α = 0° and α = 90°) in example 17.1, using Fourier voltage analysis, determine (ignore harmonics above the 10th):

i. the magnitude of the fundamental and first four harmonics
ii. the load rms voltage and current
iii. load power
iv. load power factor

Solution

The appropriate harmonic analysis is outline in the following table, for α = 0° and α = 90°.

n	Z_n	V_n (α=0)	I_n (α=0)	V_n (α=90°)	I_n (α=90°)
harmonic	$\sqrt{R^2 + (2\pi 50nL)^2}$	$\frac{0.9V_s}{n}$	V_n/Z_n	$\frac{0.9V_s}{n}\cos(\frac{1}{2}n\alpha)$	V_n/Z_n
	Ω	**V**	**A**	**V**	**A**
1	18.62	306	16.43	216.37	11.62
3	48.17	102	2.12	-72.12	-1.50
5	79.17	61.2	0.77	-43.28	-0.55
7	110.41	43.71	0.40	30.91	0.28
9	141.72	34	0.24	24.04	0.17
		332.95V	16.59A	235.43V	11.73A

i. The magnitude of the fundamental voltage is 306V for the square wave and is reduced to 216V when a phase delay angle of 90° is introduced. The table shows that the harmonics magnitudes reduce $(1/n)$ as the harmonic order increases.

ii. The rms load current and voltage can be derived by the square root of the sum of the squares of the fundamental and harmonic components, that is, for the current

$$i_{rms} = \sqrt{I_1^2 + I_3^2 + I_5^2 + \ldots\ldots}$$

The load rms currents, from the table, are 16.59A and 11.73A, which agree with the values obtained in example 17.1a. Notice that the predicted rms voltages of 333V and 235V differ significantly from the values in example 17.1a, given by $V_s\sqrt{1-\alpha/\pi}$, namely 340V and 240.4V respectively. This is because the magnitude of the harmonics higher in order than 10 are not insignificant. The error introduced into the rms current value by ignoring these higher order voltages is insignificant because the impedance increases approximately proportionally with harmonic number, hence the resultant current becomes much smaller (insignificant) as the order increases.

iii. The load power is the load i^2R loss, that is

$$P_L = i_{rms}^2 R = 16.59^2 \times 10\Omega = 2752\text{W} \quad \text{for} \quad \alpha = 0$$
$$P_L = i_{rms}^2 R = 11.73^2 \times 10\Omega = 1376\text{W} \quad \text{for} \quad \alpha = 90°$$

iv. The load power factor is the ratio of real power dissipated to apparent power, that is

$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{2752\text{W}}{16.59\text{A}\times 340\text{V}} = 0.488 \text{ for } \alpha = 0$$

$$pf = \frac{P}{S} = \frac{i_{rms}^2 R}{i_{rms} v_{rms}} = \frac{1376\text{W}}{11.79\text{A}\times 240.4\text{V}} = 0.486 \text{ for } \alpha = 90°$$

Equations (17.23) and (17.44) confirm the load power factor is 0.488, independent of α.

♣

Example 17.4: ***Single-phase half-bridge inverter with an L-R load***

A single-phase half-bridge inverter as shown in the figure 17.3, supplies a 10 Ω resistance with inductance 50 mH from a 340 V dc source. If the bridge is operating at 50 Hz, determine for the square-wave output

i. steady-state current waveforms
ii. the load rms voltage (the capacitors block any dc voltage output component)
iii. the peak load current and its time domain solution, $i_L(t)$
iv. the average and peak current in the switches
v. the average and peak current in the diodes
vi. the peak blocking voltage of each semiconductor type
vii. the power delivered to the load, rms load current, and average supply current

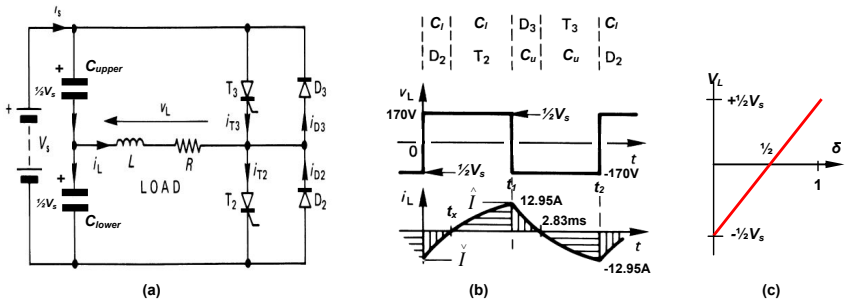


Figure 17.3. *GCT thyristor single-phase half-bridge inverter:*
(a) circuit diagram; (b) square-wave output voltage; and (c) output voltage transfer function.

Solution

From examples 17.1 and 17.2, τ = 5ms.

i. Figure 17.3 shows the output voltage and current waveforms, with various circuit component current waveforms superimposed. Note that no zero voltage loops can be created with the half-bridge. Only load voltages ±½V_s , that is ±170V dc, are possible.

ii. The output voltage swing is ±½V_s, ±170V, thus the rms output voltage is ½V_s, 170V. This is, half that of the full-bridge inverter using the same magnitude source voltage V_s, 340V dc.

iii. The peak load current is half that given by equation (17.9), that is

$$\hat{I} = \frac{½V_s}{R}\frac{1-e^{\frac{-t_1}{\tau}}}{1+e^{\frac{-t_1}{\tau}}} = \frac{½V_s}{R}\tanh\left(\frac{t_1}{2\tau}\right)$$

$$= \frac{½\times 340\text{V}}{10\Omega}\times\tanh\left(\frac{10\text{ms}}{2\times 5\text{ms}}\right) = 12.95\text{A}$$

The load current waveform is defined by equations (17.7) and (17.8), specifically

$$i_{L_I}(t) = \frac{½V_s}{R} - \left(\frac{½V_s}{R} - \check{I}\right)\times e^{\frac{-t}{\tau}}$$

$$= \frac{½\times 340\text{V}}{10\Omega} - \left(\frac{½\times 340\text{V}}{10\Omega} + 12.95\text{A}\right)\times e^{\frac{-t}{5\text{ms}}}$$

$$= 17 - 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

and

$$i_{L_{II}}(t) = -\frac{½V_s}{R} + \left(\frac{½V_s}{R} + \hat{I}\right)\times e^{\frac{-t}{\tau}}$$

$$= -\frac{½\times 340\text{V}}{10\Omega} + \left(\frac{½\times 340\text{V}}{10\Omega} + 12.95\right)\times e^{\frac{-t}{5\text{ms}}}$$

$$= -17 + 29.95\, e^{\frac{-t}{5\text{ms}}} \qquad \text{for} \qquad 0 \le t \le 10\text{ms}$$

By halving the effective supply voltage, the current swing is also halved.

iv. The peak switch current is $\hat{I} = 12.95\text{A}$.
The average switch current is given by

$$\bar{I}_T = \frac{1}{20\text{ms}}\int_{2.83\text{ms}}^{10\text{ms}} (17 - 29.95e^{\frac{-t}{5\text{ms}}})\, dt$$

$$= 2.86\text{ A}$$

v. The peak diode current is $\hat{I} = 12.95\text{A}$.
The average diode current is given by

$$\bar{I}_D = \frac{1}{20\text{ms}}\int_{0}^{2.83\text{ms}} \left(17 - 29.95e^{\frac{-t}{5\text{ms}}}\right) dt$$

$$= 0.83\text{ A}$$

vi. When a switch or diode of a parallel pair conduct, the complementary pair of devices experience a voltage V_s, 340V dc. Thus although the load experiences half the supply voltage, the semiconductors experience twice that voltage, the same voltage experienced by the switches in the full bridge inverter.

vii. The load power (whence various currents) is found by averaging the instantaneous load power

$$P_L = \frac{1}{10\text{ms}}\int_0^{10ms} 170\text{V}\times\left(17 - 29.95\times e^{-200t}\right) dt \qquad i_{rms} = \sqrt{P_L/R} \qquad \bar{I}_s = P_L/V_s$$

$$= 638.5\text{ W} \qquad = \sqrt{638.5\text{W}/10\Omega} = 8\text{A} \qquad = 638.5\text{W}/340\text{V} = 1.88\text{A}$$

♣

17.1.1iii - PWM-wave output

The output voltage and frequency of a single-phase voltage-source inverter bridge can be control using one of two forms of pulse-width modulation, termed:

- bipolar
- multi-level, usually (meaninglessly) called unipolar

Both pwm techniques have been analysed extensively for dc voltage outputs when applied to the two quadrant and four quadrant dc choppers considered in Chapter 16, sections 16.5 and 16.6. It will be seen that the same triangular modulation principles can be applied and extended, when producing low-harmonic single-phase ac output voltages and currents. The main voltage output difference between the two methods is the harmonic content near the carrier frequency and its harmonics. Three-phase pwm is a naturally extension to the single-phase case, except single-phase pwm offers more degrees of flexibility than its application to three phase inverters, although three-phase pwm does have the attribute of triplen harmonic cancellation, due to the use of one (co-phasal) triangular carrier.

Bipolar pulse width modulation

Bipolar modulation is the simplest pwm method and involves comparing a fixed frequency and magnitude triangular carrier with the ac waveform desired, called the modulation waveform. The modulation waveform is usually a sinusoid of magnitude (modulation index) M such that $0 \le M \le 1$.
The waveforms in figure 17.4 shown that the load voltage V_L swings between the two voltage levels, $+V_s$ and $-V_s$, (hence the term bipolar output voltage), according to

- T_1 and T_2 are on when $v_{ref} > v_\Delta$ (T_3 and T_4 are off) such that $V_L = +V_s$
- T_3 and T_4 are on when $v_{ref} < v_\Delta$ (T_1 and T_2 are off) such that $V_L = -V_s$

Multi-level pulse width modulation

Two multilevel output voltage techniques can be use with single-phase voltage fed ac bridges. In both case, two triangular carries displaced by 180° give the same output for the same switching frequency.

i. The waveforms in figure 17.5 show that the load voltage V_L swings between the two voltage levels, $+V_s$ and $-V_s$, with interspaced zero periods (hence the term multilevel, specifically three-level in this case, 0V and $\pm V_s$), according to

- T_1 is on when $v_{ref} > v_\Delta$ such that $V_{ao} = +V_s$
- T_4 is on when $v_{ref} < v_\Delta$ such that $V_{ao} = 0V$

- T_3 is on when $v_{ref} < -v_\Delta$ such that $V_{bo} = V_s$
- T_2 is on when $v_{ref} > -v_\Delta$ such that $V_{bo} = 0V$

The multilevel load output voltage is the difference between the two leg voltage waveforms and can be defines as follows:

- T_1 and T_2 are on such that $V_{ao} = +V_s$, $V_{bo} = 0V$, $V_{ab} = +V_s$
- T_2 and T_3 are on such that $V_{ao} = 0V$, $V_{bo} = +V_s$, $V_{ab} = -V_s$

- T_1 and T_3 are on such that $V_{ao} = +V_s$, $V_{bo} = +V_s$, $V_{ab} = 0V$
- T_2 and T_4 are on such that $V_{ao} = 0V$, $V_{bo} = 0V$, $V_{ab} = 0V$

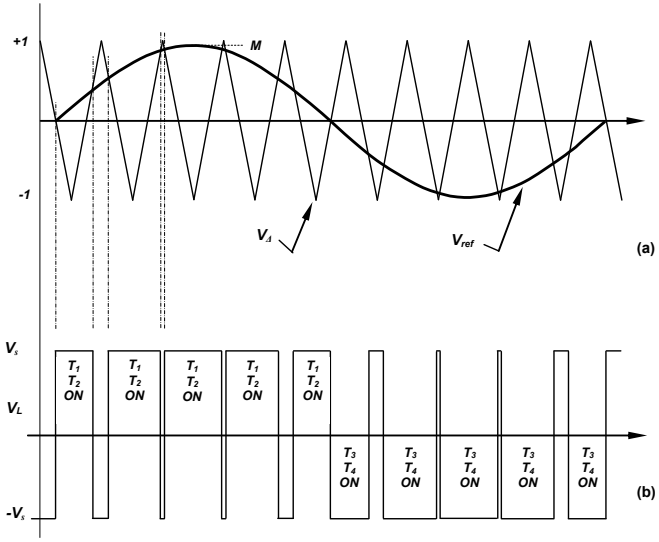


Figure 17.4. *Bipolar pulse width modulation: (a) carrier and modulation waveforms and (b) resultant load pwm waveform.*

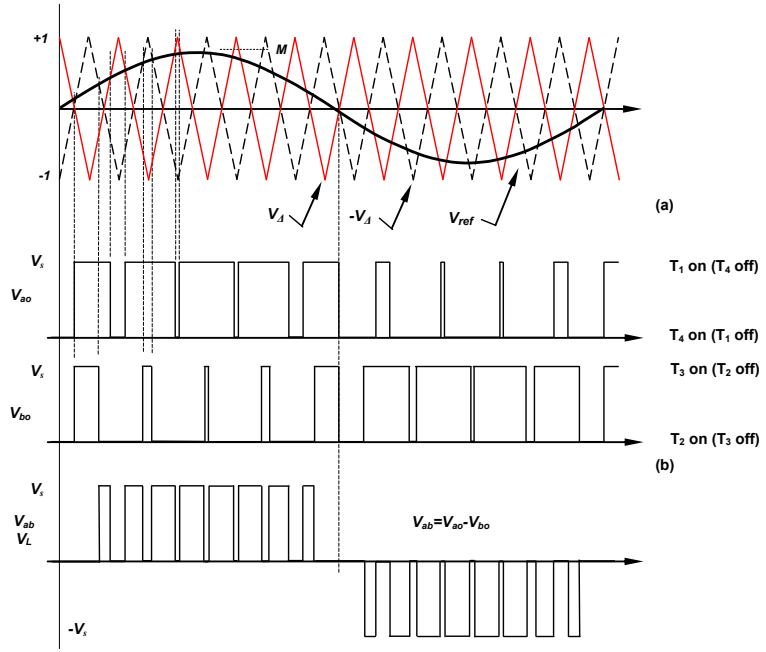


Figure 17.5. *Multilevel (3 level) pulse width modulation: (a) carriers and modulation waveforms and (b) resultant load pwm waveforms.*

The two zero output states are interleaved to balance switching losses between all four bridge switches. Device switching is at the carrier frequency, but the bridge load voltage (hence load current) experiences twice the leg switching frequency since the two carriers are displaced by 180°.

ii. A second multilevel output voltage approach is shown in figure 17.17, where the triangular carriers are not only displaced by 180° in time, but are vertically displaced, as for multilevel inverter pwm generation, which is considered in section 17.4 (half the magnitude and twice the frequency as in figure 17.6). The upper triangle modulates reference values greater than zero, while the lower triangle modulates when the reference is less than zero.

Spectral comparison between bipolar and multilevel pwm waveforms

The key features of the H-bridge inverter output voltage with bipolar pwm are (fig 17.6a):

- a triangular carrier has only odd Fourier components, so the output spectrum only has carrier components at odd harmonics of the carrier frequency
- the first carrier components occur at the carrier frequency, $\boldsymbol{f_c}$
- side-band components occur spaced by $\boldsymbol{2f_o}$ from other components, around all multiples of the carrier frequency $\boldsymbol{f_c}$

From figure 17.6b, the key features of the H-bridge inverter output voltage with multilevel pwm are:

- the output switching frequency is double $\boldsymbol{2f_c}$ each leg switching frequency $\boldsymbol{f_c}$, since the switching of each leg is time shifted (by 180°), hence the first carrier related components in the output occur at $\boldsymbol{2f_c}$ and then at multiples of $\boldsymbol{2f_c}$ (effectively the carrier is $2f_o$)
- no triangular carrier Fourier components exist in the output voltage since the two carriers are in anti-phase (180° apart), effectively cancelling one another in spectrum terms
- side-band components occur spaced by $\boldsymbol{2f_o}$ from other components, around each multiple of the carrier frequency $\boldsymbol{2f_c}$

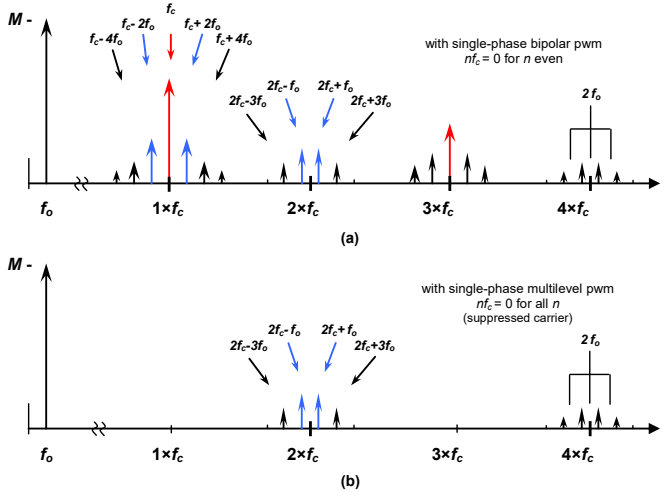


Figure 17.6. *Typical phase output frequency spectrum, at a give switch commutation frequency, for: (a) bipolar pwm and (b) multilevel pwm.*

17.1.2 Three-phase voltage-source inverter bridge

The basic dc to three-phase voltage-source inverter (VSI) bridge is shown in figure 17.7. It comprises six power switches together with six associated reactive energy feedback diodes. Each of the three inverter legs operates at a relative time displacement (phase) of ⅔π, 120°.

Table 17.1: Quasi-square-wave six conduction states - *180° conduction*

Interval	***Three** conducting switches*								*leg state*	*voltage vector*
1	T_1	T_2	T_3						101	v_5
2		T_2	T_3	T_4					001	v_1
3			T_3	T_4	T_5				011	v_3
4				T_4	T_5	T_6			010	v_2
5					T_5	T_6	T_1		110	v_6
6						T_6	T_1	T_2	100	v_4

17.1.2i - 180° (π) conduction

Figure 17.8 shows inverter bridge quasi-square output voltage waveforms for a 180° switch conduction pattern. Each switch conducts for 180°, such that no two series connected (leg or arm) semiconductor switches across the voltage rail conduct simultaneously. Six patterns exist for one output cycle and the rate of sequencing these patterns, $6f_o$, specifies the bridge output frequency, f_o. The conducting switches during the six distinct intervals are shown and can be summarised as in Table 17.1.

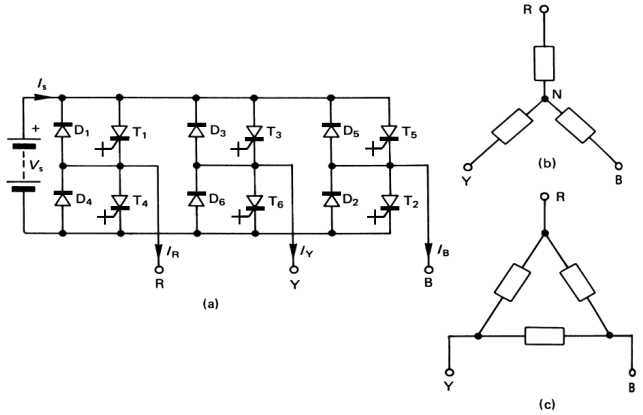


Figure 17.7. *Three-phase VSI inverter circuit:*
(a) GCT thyristor bridge inverter; (b) star-type load; and (c) delta-type load.

The three output voltage waveforms can be derived by analysing a balanced resistive star load and considering each of the six connection patterns, as shown in figure 17.9, using the matrix in figure 17.8c. Effectively the resistors representing the three-phase load are sequentially cycled anticlockwise one at a time, being alternately connected to each supply rail. The output voltage is independent of the load, as it is for all voltage source inverters.

Alternatively, the generation of the three-phase voltages can be analysed analytically by using the rotating *voltage space vector* technique. With this approach, the output voltage state from each of the three inverter legs (or poles) is encoded as summarised in table 17.1, where a '1' signifies the upper switch in the leg is on, while a '0' means the lower switch is on in that leg. The resultant binary number (one bit for each of the three inverter legs), represents the output voltage vector number (when converted to decimal). The six voltage vectors are shown in figure 17.10 forming sextant boundaries, where the quasi-square output waveform in figure 17.8b is generated by stepping instantaneously from one vector position to another in an anticlockwise direction. Note that the rotational stepping sequence is arranged such that when rotating in either direction, only one leg changes state, that is, one device turns off and then the complementary switch of that leg turns on, at each step. This minimises the inverter switching losses. The dwell time of the created rotating vector at each of the six vector positions, is ⅓π ($\frac{1}{6}T$) of the cycle period (T). Note that the line-to-line zero voltage states 000 and 111 are not used. These represent the condition when ***either*** all the upper switches (T_1, T_3, T_5) are on ***or*** all the lower switches (T_2, T_4, T_5) are switched on (represented as the origin in figure 17.10). Phase reversal can be obtained by interchanging two phase outputs, or as is the preferred method, the direction of the rotating vector sequence is reversed. Reversing is therefore effectively achieved by back-tracking along each output waveform.

With reference to figure 17.8b, the line-to-load neutral voltage Fourier coefficients are given by

$$V_{n_{L-N}} = \frac{2}{3\pi} V_s \frac{2 + \cos\frac{n\pi}{3} - \cos\frac{2n\pi}{3}}{n} \tag{17.45}$$

The line-to-load neutral voltage is therefore

$$V_{n_{L-N}} = \frac{2}{\pi} V_s \sum_{n=1,6r\pm1}^{\infty} \frac{\sin n\omega t}{n} \qquad r = 1, 2, 3, .. \tag{17.46}$$

that is

$$v_{RN} = \frac{2}{\pi} V_s \left[\sin\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ \ldots\right] \quad \text{(V)} \tag{17.47}$$

similarly for v_{YN} and v_{BN}, where ωt is substituted by ωt+⅔π and ωt-⅔π respectively.

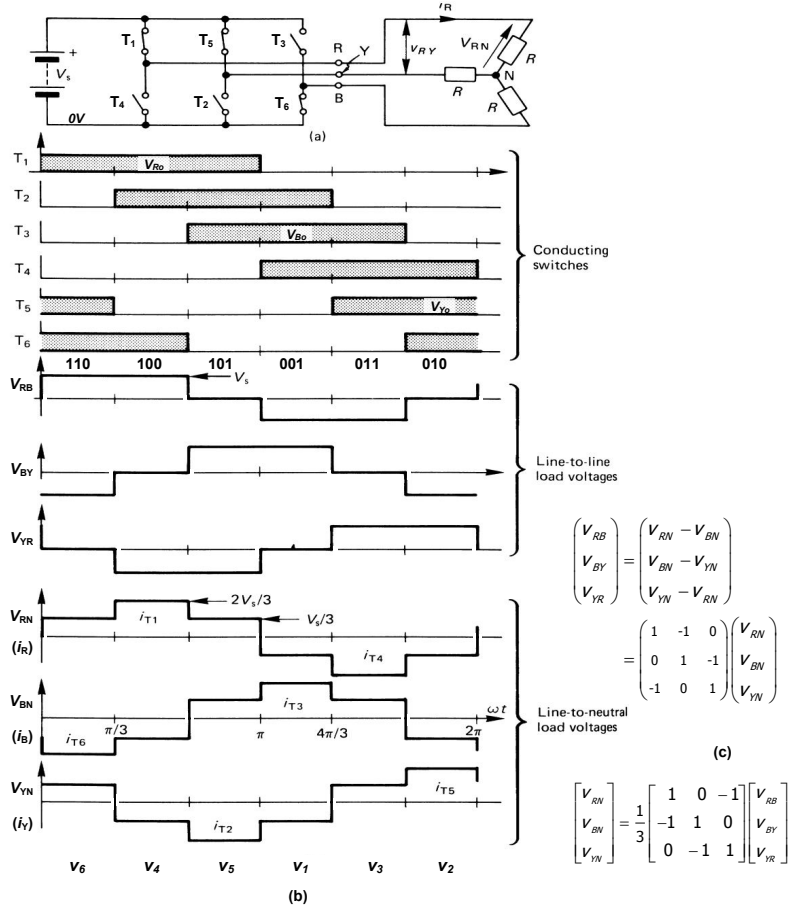


Figure 17.8. *A three-phase bridge inverter employing 180° switch conduction with a resistive load: (a) the bridge circuit showing T_1, T_5, and T_6 conducting (leg state **v_6 :– 110**); (b) circuit voltage and current waveforms with each of six sequential output voltage vectors identified; and (c) phase voltage to line voltage conversion matrices and vice versa.*

The line-to-line voltage, from equation (17.38) with α = ⅓π, gives Fourier coefficients defined by

$$V_{n_{L-L}} = \frac{4}{\pi} V_s \frac{\left(\cos\frac{n\pi}{6}\right)}{n} \tag{17.48}$$

The line-to-line voltage is thus

$$V_{n_{L-L}} = \frac{2\sqrt{3}}{\pi} V_s \sum_{n=1,6r\pm1}^{\infty} \left\| \cos\frac{n\pi}{6} \right\| \frac{\sin n\omega t}{n} \qquad r = 1, 2, 3, . \qquad (17.49)$$

(the $\| \ \|$ symbol provides the sign), that is

$$v_{RB} = \frac{2\sqrt{3}}{\pi} V_s \left[\sin\omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots \right] \quad (V) \qquad (17.50)$$

and similarly for v_{BY} and v_{YR}. Figure 17.8b shows that v_{RB} is shifted $\frac{1}{6}\pi$ with respect to v_{RN}, hence to obtain the three line voltages while maintaining a v_{RN} reference, ωt should be substituted with $\omega t + \frac{1}{6}\pi$, $\omega t - \frac{1}{2}\pi$ and $\omega t + \frac{5}{6}\pi$, respectively. The three line-to-line fundamental voltages are:

$$V_{AB,1} = \frac{2\sqrt{3}}{\pi} V_s \sin\left(\omega t + \tfrac{1}{6}\pi\right)$$

$$V_{BC,1} = \frac{2\sqrt{3}}{\pi} V_s \sin\left(\omega t - \tfrac{1}{2}\pi\right)$$

$$V_{CA,1} = \frac{2\sqrt{3}}{\pi} V_s \sin\left(\omega t + \tfrac{5}{6}\pi\right)$$

Since the interphase voltages consist of two square waves displaced by $\frac{2}{3}\pi$, no triplen harmonics (3, 6, 9, . . .) exist. The outputs comprise harmonics given by the series $n = 6r \pm 1$ where $r \geq 0$ and is an integer. The nth harmonic has a magnitude of $1/n$ relative to the fundamental.

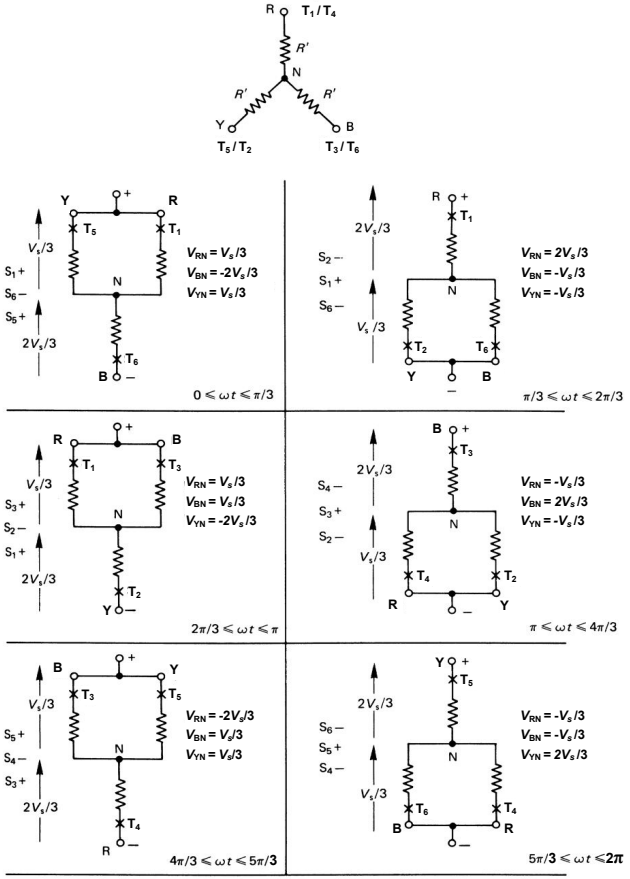


Figure 17.9. *Determination of the line-to-neutral voltage waveforms for a balanced resistive load and 180° conduction as illustrated in figure 17.8.*

By examination of the interphase output voltages in figure 17.8 it can be established that the mean half-cycle voltage is $\frac{2}{3}V_s$ and the rms value is $\sqrt{\frac{2}{3}}\,V_s$, namely 0.816 V_s. From equation (17.50) the rms value of the fundamental is $\sqrt{6}\,V_s/\pi$, namely 0.78 V_s, that is 3/π times the total rms voltage value.
The three-phase inverter output voltage properties are summarised in Table 17.2.

17.1.2ii - 120° (⅔π) conduction

The basic three-phase inverter bridge in figure 17.7 can be controlled with each switch conducting for 120°. As a result, at any instant only two switches (one upper and one non-complementary lower) conduct and the resultant quasi-square output voltage waveforms are shown in figure 17.12. A 60° (⅓π), dead time exists between two series switches conducting, thereby providing a safety margin against *simultaneous conduction* of the two series devices (for example T_1 and T_4) across the dc supply rail. This safety margin is obtained at the expense of a lower semi-conductor device utilisation and rms output voltage than with 180° device conduction. The device conduction pattern is summarised in Table 17.3. A feature with ⅔π conduction is that the phase currents can be measured from the dc link current.

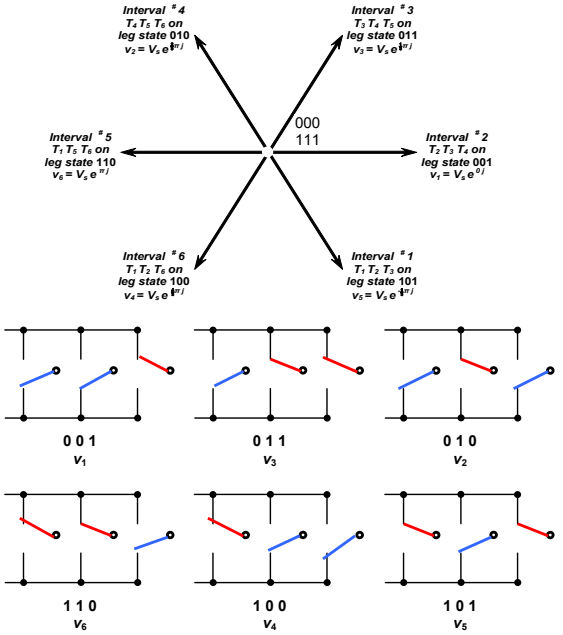


Figure 17.10. *Generation and arrangement of the six quasi-square inverter output voltage states.*

Figure 17.8b for 180° conduction and 17.12b for 120° conduction show that the line to neutral voltage of one conduction pattern is proportional to the line-to-line voltage of the other. That is, from equation (17.38) with $\alpha = \frac{1}{3}\pi$

$$v_{RN}\left(\tfrac{2}{3}\pi\right) = \tfrac{1}{2}v_{RY}\left(\pi\right) = \sum_{n=1,3,5}^{\infty} \frac{2}{\pi n} V_s \cos\frac{n\pi}{6}\sin n\omega t$$

$$= \frac{\sqrt{3}}{\pi} V_s \left[\sin\omega t - \tfrac{1}{5}\sin 5\omega t - \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots \right] \quad (V) \qquad (17.51)$$

and

$$v_{RY}\left(\tfrac{2}{3}\pi\right) = \tfrac{3}{2}v_{RN}\left(\pi\right) = \sum_{n=1,3,5}^{\infty} \frac{2\sqrt{3}}{\pi n} V_s \cos\frac{n\pi}{6}\sin n\omega t$$

$$= \frac{3}{\pi} V_s \left[\sin\omega t + \tfrac{1}{5}\sin 5\omega t + \tfrac{1}{7}\sin 7\omega t + \tfrac{1}{11}\sin 11\omega t + \ldots \right] \quad (V) \qquad (17.52)$$

Also $v_{RY} = \sqrt{3}\,v_{RN}$ and the phase relationship between these line and phase voltages, of $\frac{1}{6}\pi$, has not been retained. That is, with respect to figure 17.12b, substitute ωt with $\omega t + \frac{1}{6}\pi$ in equation (17.51) and $\omega t + \frac{1}{3}\pi$ in equation (17.52). 180° conduction gives a 15% increase in ac voltage magnitude compared to 120° conduction, but both techniques give the same harmonic spectrum components.

The output voltage properties for both 120° and 180° conduction are summarised in the Table 17.2.

Independent of the conduction angle (120°, 180° or even 150°), quasi-square 180° conduction occurs with inductive loads, producing the six hexagon states shown in the upper part of figure 17.10. The resistive load assumptions made in this section for explanation purposes can be misleading.

Table 17.2: Quasi-squarewave voltage properties for a resistive load

Conduction period	Fundamental voltage		Characteristic		
	peak	rms	Total rms	Distortion Factor	THD
	$\hat{V}_1$	V_1	V_{rms}	μ	thd
180°	(V)	(V)	(V)		
Phase Voltage $V_{L\text{-}N}$	$\frac{2}{\pi}V_s = 0.637V_s$	$\frac{\sqrt{2}}{\pi}V_s = 0.450V_s$	$\frac{\sqrt{2}}{3}V_s = 0.471V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{2\sqrt{3}}{\pi}V_s = 1.10V_s$	$\frac{\sqrt{6}}{\pi}V_s = 0.78V_s$	$\sqrt{\frac{2}{3}}V_s = 0.816V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
120°	(V)	(V)	(V)		
Phase Voltage $V_{L\text{-}N}$	$\frac{\sqrt{3}}{\pi}V_s = 0.551V_s$	$\frac{\sqrt{6}}{2\pi}V_s = 0.390V_s$	$\frac{1}{\sqrt{6}}V_s = 0.408V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$
Line Voltage $V_{L\text{-}L}$	$\frac{3}{\pi}V_s = 0.955V_s$	$\frac{3}{\sqrt{2}\pi}V_s = 0.673V_s$	$\frac{1}{\sqrt{2}}V_s = 0.707V_s$	$\frac{3}{\pi} = 0.955$	$\sqrt{\frac{\pi^2}{9}-1} = 0.311$

Table 17.3: Quasi-squarewave conduction states - *120° conduction*

Interval	***Two** conducting devices*						
1	T_1	T_2					
2		T_2	T_3				
3			T_3	T_4			
4				T_4	T_5		
5					T_5	T_6	
6						T_6	T_1

An ideal switch model of the three-phase voltage source inverter, with 180° conduction, connected to passive load, where (T_1, T_4), (T_5, T_2) and (T_3 and T_6) represent complementary switch pairs, can be describe by: $T_1+T_4=1$; $T_5+T_2=1$ and $T_3+T_6=1$. The upper and lower switches in the same arm operate in a complementary manner, that is, turning on T_1 corresponds to $T_1=1$ and $T_4=0$, and similarly phases Y and B. Then the inverter terminal voltages at R, Y and B relative to supply mid-point 'o' can be synthesized from dc link voltage as:

$$v_{Ro} = ½(T_1\text{-}T_4)V_s$$
$$v_{Yo} = ½(T_5\text{-}T_2)V_s$$
$$v_{Bo} = ½(T_3\text{-}T_6)V_s$$

With T_1 on and T4 off, the converter output phase R is connected to $½V_s$, while T_1 off and T_4 on connects output phase R to $-½V_s$.
The equations describing the ac side transients for a three-phase load R_R, R_Y, R_B, and L_R, L_Y, L_B are:

$$\frac{d}{dt}\begin{bmatrix} i_R \\ i_Y \\ i_B \end{bmatrix} = \begin{bmatrix} \frac{v_{Rn}}{L_R} \\ \frac{v_{Yn}}{L_Y} \\ \frac{v_{Bn}}{L_B} \end{bmatrix} - \begin{bmatrix} \frac{R_R}{L_R} & 0 & 0 \\ 0 & \frac{R_Y}{L_Y} & 0 \\ 0 & 0 & \frac{R_B}{L_B} \end{bmatrix} \begin{bmatrix} i_R \\ i_Y \\ i_B \end{bmatrix}$$

where v_{Rn}, v_{Yn} and v_{Bn} are phase voltages relative to the load floating neutral-point '*n*', where $i_R+i_Y+i_B=0$.

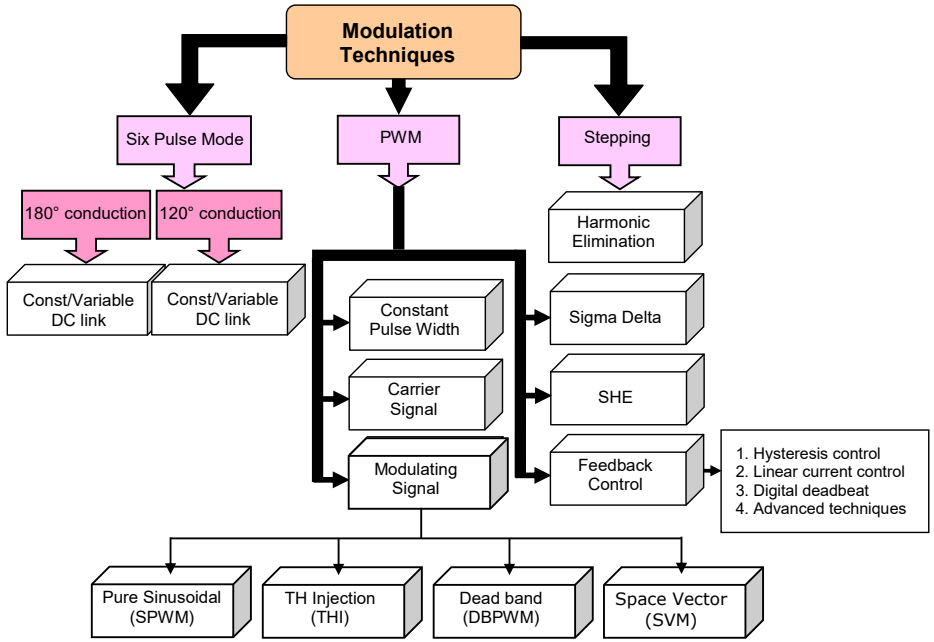


Figure 17.11. *Derivation tree for three-phase bridge inverter output frequency and magnitude control techniques.*

17.1.3 Inverter ac output voltage and frequency control techniques

It is a common requirement that the output voltage and/or frequency of an inverter be varied in order to control the load power or, in the case of an induction motor, to control the shaft speed and torque by maintaining a constant *V/f* ratio. The six VSI modulation control techniques to be considered are:

- Variable voltage dc link
- Single-pulse width modulation
- Multi-pulse width modulation
- Multi-pulse, selected notching modulation
- Sinusoidal pulse width modulation
- Triplen injection
  - Triplens injected into the modulation waveform
  - Voltage space vector modulation
- Selected harmonic elimination, SHE

Inverter voltage and frequency control techniques are summarised in figure 17.11.

17.1.3i - Variable voltage dc link

The rms voltage of a square-wave can be changed and controlled by varying the dc link source voltage. A *variable dc link* voltage can be achieved with a dc chopper as considered in chapter 16 or an ac phase-controlled thyristor bridge as considered in sections 14.2 and 14.4. A dc link *L-C* smoothing filter may be necessary.

17.1.3ii - Single-pulse width modulation

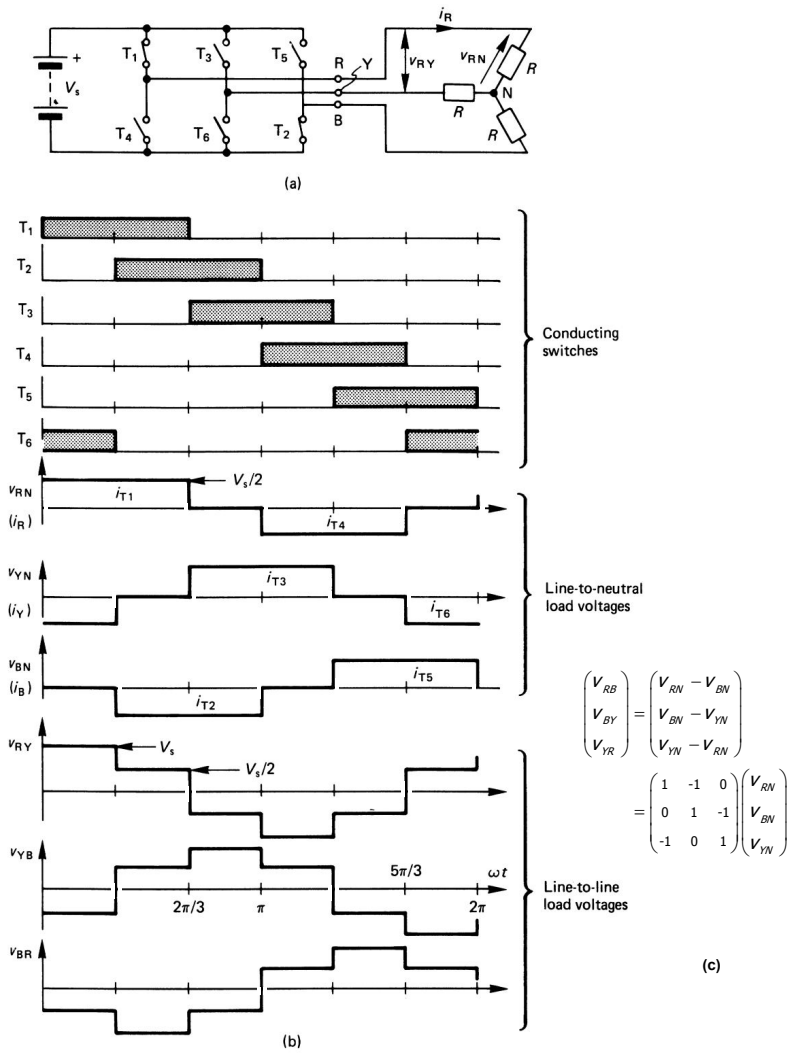
Simple pulse-width control can be employed as considered in section 17.1.1b, where a single-phase bridge is used to produce a quasi-square-wave output voltage as shown in figure 17.1c.
An alternative method of producing a quasi-square wave of controllable pulse width is to transformer-add the square-wave outputs from two push-pull bridge inverters as shown in figure 17.13a. By phase-shifting the output by α, a quasi-square sum results as shown in figure 17.13b.

The output voltage can be described by

$$V_o = \sum_{n\ odd}^{\infty} v_{an} \sin n\omega t \qquad \text{(V)} \qquad (17.53)$$

where

$$v_{an} = \frac{2}{\pi}\int_{-½\pi}^{½\pi} V_s \cos n\alpha\, d\alpha = \frac{4}{n\pi} V_s \cos(½n\alpha) \qquad \text{(V)} \qquad (17.54)$$



$$\begin{pmatrix} V_{RB} \\ V_{BY} \\ V_{YR} \end{pmatrix} = \begin{pmatrix} V_{RN} - V_{BN} \\ V_{BN} - V_{YN} \\ V_{YN} - V_{RN} \end{pmatrix} = \begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{pmatrix} \begin{pmatrix} V_{RN} \\ V_{BN} \\ V_{YN} \end{pmatrix}$$

Figure 17.12. *A three-phase bridge inverter employing 120° switch conduction with a resistive star load: (a) the bridge circuit showing T_1 and T_2 conducting; (b) circuit voltage and current waveforms; and (c) phase voltage to line voltage conversion matrix.*

The rms output voltage is

$$V_r = V_s\sqrt{1 - \alpha/\pi} \qquad \text{(V)} \qquad (17.55)$$

and the rms value of the fundamental is

$$V_1 = \frac{2\sqrt{2}}{\pi} V_s \cos ½\alpha \qquad \text{(V)} \qquad (17.56)$$

As α increases, the magnitude of the harmonics, particularly the third, becomes significant compared with the fundamental magnitude. This type of control may be used in high power applications.

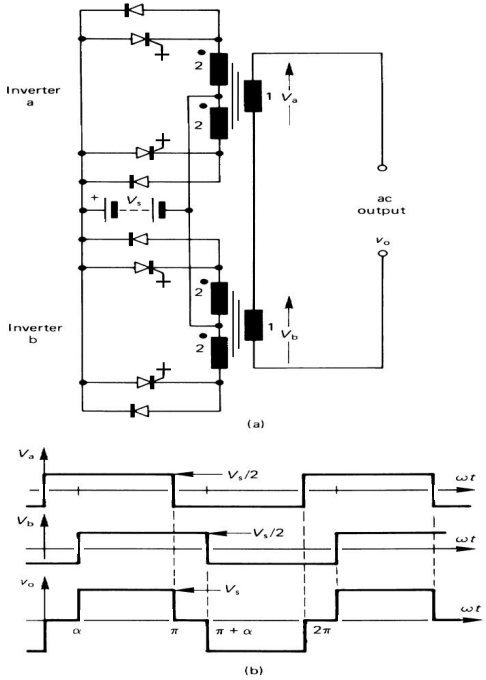


Figure 17.13. *Voltage control by combining phase-shifted push-pull inverters: (a) two inverters with two transformers for summing and (b) circuit voltage waveforms for a phase displacement of α.*

Example 17.5: ***Single-pulse width modulation***

Two single-phase H-bridge inverter outputs are transformer added, as shown in figure 17.13. Each inverter operates at 50Hz but phase shifted so as to produce 240V rms fundamental output when the rail voltage of each inverter is 340V dc and the transformers turns ratios are 2:2:1.

Determine

i. the phase shift between the two single phase inverters
ii. the rms output voltage
iii. the frequency and magnitude of the first 4 harmonics of 50Hz and their rms ac contribution to the rms output
iv. rms voltage of higher order harmonics (higher frequencies than those in part iii.)
v. the total harmonic distortion of the output voltage.

Solution

i. The output is a quasi-square waveform of magnitude ±340V dc. The magnitude of the 50Hz fundamental is given by equation (17.54), for n =1:

$$v_{a1} = \frac{4}{\pi} V_s \cos(½\alpha)$$

$$\sqrt{2}\ 240\text{V} = \frac{4}{\pi} \times 340\text{V} \times \cos(½\alpha)$$

from which the phase shift is 76.7°, 1.34 radians.

ii. The rms output voltage is given by equation (17.55), that is

$$V_{rms} = V_s\sqrt{1 - \alpha/\pi} = 340\text{V}\sqrt{1 - 1.34/\pi} = 257.5\text{V}$$

iii. The peak values of the first four harmonics are given in the table below.

harmonic n	$v_{an} = \frac{4}{n\pi}V_s \cos(½n\alpha)$	v_{an}^2
3	-61.4	3765.0
5	-84.7	7175.3
7	-1.4	1.9
9	46.6	2168.5
	$\sqrt{\sum v_{an}^2} =$	114.50

The rms value of the ac of the first four harmonics is 114.5/√2 = 81.0V.

iv. The ac component of the harmonics above the 9th is given by

$$V_{rms\ n>9} = \sqrt{V_{rms}^2 - V_{rms\ n\le 9}^2}$$
$$= \sqrt{257.5\text{V}^2 - \left(240\text{V}^2 + 81.0\text{V}^2\right)} = 46.3\text{V}$$

v. The total harmonic voltage distortion is given by

$$THD_v = \frac{\sqrt{V_{rms}^2 - V_{a1}^2}}{V_{a1}} \times 100 = \sqrt{\left(\frac{V_{rms}}{V_{a1}}\right)^2 - 1} \times 100$$
$$= \sqrt{\left(\frac{257.5\text{V}}{240\text{V}}\right)^2 - 1} \times 100 = 38.9\%$$

♣

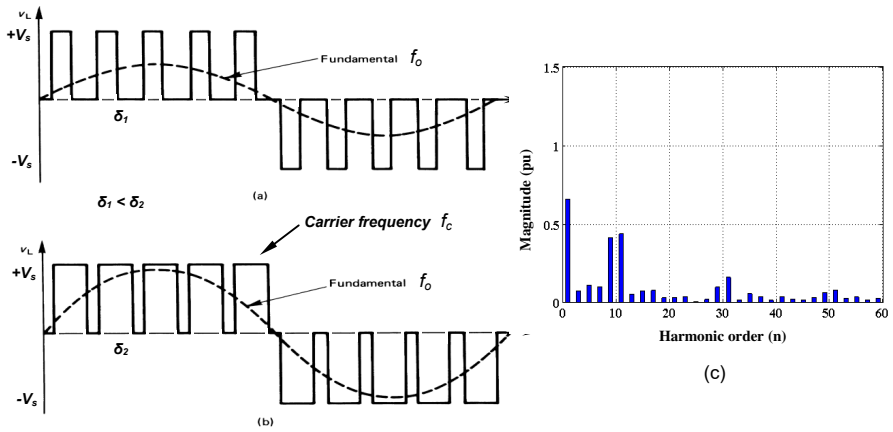


Figure 17.14. *Inverter control giving variable duty cycle of five notches per half cycle: (a) low duty cycle, δ_1, hence low fundamental magnitude, (b) higher duty cycle, δ_2, for a high fundamental voltage output, and (c) voltage output spectrum.*

17.1.3iii - Multi-pulse width modulation

An extension of the single-pulse modulation technique is multiple-notching as shown in figure 17.14. The bridge switches are controlled so as to vary the on to off time of each notch, δ, thereby varying the output rms voltage which is given by $V_{rms} = \sqrt{\delta}V_s$. Alternatively, the number of notches can be varied.

The harmonic content at lower output voltages is significantly lower than that obtained with single-pulse modulation. The increased switching frequency does increase the magnitude of higher order harmonics and the switching losses. The Fourier coefficients of the output voltage in figure 17.14 are given by

$$V_n = \frac{4}{n\pi}\sum_{j=1,2,3,..}^{f_c/f_o}\left[\cos 2\pi\frac{f_o}{f_c}n\left(2j - 1 + \delta\right) - \cos 2\pi\frac{f_o}{f_c}n\left(2j - 1 - \delta\right)\right] \quad (17.57)$$

where f_o is the fundamental frequency, f_c the triangular carrier frequency and $0 \le \delta \le 1$ is the duty cycle.

17.1.3iv - Multi-pulse, selected notching modulation – selected harmonic elimination

If a multi-level waveform ($\pm V_s$, 0) is used with quarter wave symmetry, as shown in figure 17.15a, then both the harmonics and total rms output voltage can be controlled. With one pulse per quarter wave, the k^{th} harmonic is eliminated from the output voltage if the centre of the pulse is located such that

$$\sin k\lambda = 0$$
$$\text{that is } \lambda = \pi/k \quad (17.58)$$

Independent of the pulse width δ, the k^{th} harmonic is eliminated and the other Fourier components are given by

$$V_n = \frac{8}{n\pi}V_s \sin n\frac{\pi}{k} \sin n\delta \quad (17.59)$$

The output voltage total rms is solely dependent on the pulse width δ and is given by

$$V_{o\,rms} = V_s\sqrt{\frac{2}{\pi}\delta} \quad (17.60)$$

On the other hand, the bipolar waveform ($\pm V_s$) in figure 17.15b has an rms value of V_s, independent of the harmonics eliminated.

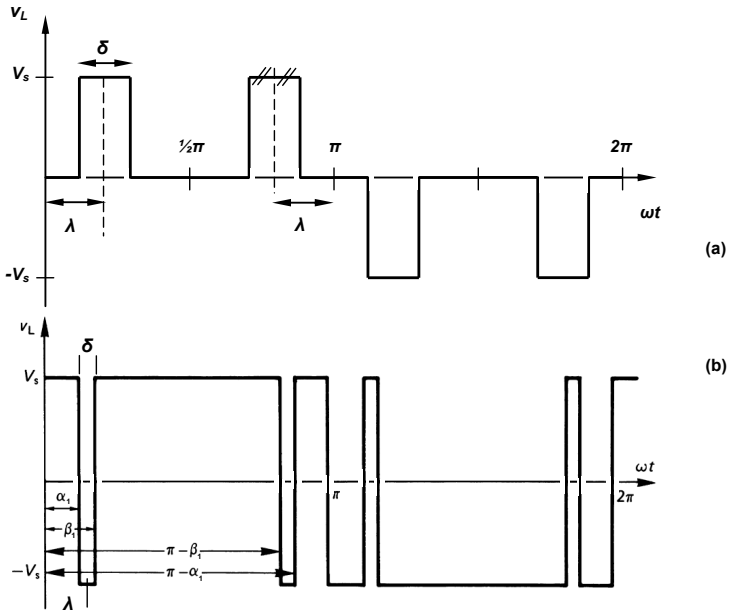


Figure 17.15. *Output voltage harmonic reduction for a single-phase bridge using selected notching: (a) multilevel output voltage and (b) bipolar output voltage.*

Selected elimination of lower-order harmonics can be achieved by producing an output voltage waveform as shown in figure 17.15b. The exact switching points are calculated off-line so as to eliminate the required harmonics. For n switchings per half cycle, n selected harmonics can be eliminated.

In figure 17.15b two notches per half cycle are introduced; hence any two selected harmonics can be eliminated. The more notches, the lower is the output fundamental. For example, with two notches, the third and fifth harmonics are eliminated. From

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f(\theta)\sin n\theta\, d\theta \quad \text{for} \quad n = 1, 2, 3, ... \tag{17.61}$$

$$b_3 = \frac{4}{3\pi}V_s\left(1 - 2\cos 3\alpha + 2\cos 3\beta\right) = 0$$

and

$$b_5 = \frac{4}{5\pi}V_s\left(1 - 2\cos 5\alpha + 2\cos 5\beta\right) = 0$$

Solving yields α_1 = 23.6° and β_1 = 33.3°. The total rms output voltage is V_s, independent of the harmonics eliminated. The magnitude (whence rms) of each harmonic component is

$$V_n = \frac{4}{n\pi}V_s\left(1 - 4\times\sin n\lambda \times \sin n\delta\right) \tag{17.62}$$

The maximum fundamental rms component of the output voltage waveform is 0.84 of a square wave, which is $(2\sqrt{2}/\pi)V_s$ when $\delta = \pi/2$ which produces a square wave.
Ten switching intervals exist compared with two per cycle for a square-wave, hence switching losses and control circuit complexity are increased.

In the case of a three-phase inverter bridge, the third harmonic does not exist, hence the fifth and seventh (b_5 and b_7) can be eliminated with α_1 = 16.3° and β_1 = 22.1. The 5th, 7th, 11th, and 13th can be eliminated with the angles 10.55°, 16.09°, 30.91°, and 32.87° respectively. Because the waveforms have quarter wave symmetry, only angles for 90° need be stored.

The output rms voltage magnitude can be varied by controlling the dc link voltage or by transformer-adding two phase-displaced bridge outputs as demonstrated in figure 17.13. The output voltage Fourier components in equation (17.62) are modified by equation(17.54) given

$$V_n = \frac{4}{n\pi}V_s\left(1 - 4\times\sin n\lambda \times \sin n\delta\right)\cos \tfrac{1}{2}n\alpha \tag{17.63}$$

And the total rms output voltage is reduced from V_s , as given by equation (17.55), that is

$$V_{oms} = V_s\sqrt{1 - \alpha/\pi} \qquad \text{(V)} \tag{17.64}$$

Thus the fundamental rms magnitude can be changed by introducing an extra constraint to be satisfied, along with the harmonic eliminating constraints (as a result of the extra constraint, one fewer harmonic can now be eliminated for a given number of switchings per quarter cycle).

The multi-pulse selected notching modulation technique can be extended to the *optimal pulse-width modulation method,* where harmonics may not be eliminated, but minimised according to a specific criterion. In this method, the quarter wave output is considered to have a number of switching angles. These angles are selected so as, for example, to eliminate certain harmonics, minimise the rms of the ripple current, or any other desired performance index. The resultant non-linear equations are solved using numerical methods off-line. The computed angles are then stored in a ROM look-up table for use. A set of angles must be computed and stored for each desired level of the voltage fundamental and output frequency.
The optimal pwm approach is particularly useful for high-power, high-voltage GCT thyristor inverters, which tend to be limited in switching frequency by device switching losses.

Generally *sinωt+ksin3ωt* is generated (since the third harmonic of the square wave is not eliminated)

$$b_n = \frac{4}{\pi}\int_0^{\pi/2} f(\theta)\sin n\theta\, d\theta = \frac{4}{\pi}\int_0^{\pi/2} 1\times\sin n\theta\, d\theta$$

For a fundamental magnitude of √3m of the pu link voltage and to eliminate *N*-1 (*N*-1>2) harmonics:

$$\begin{aligned} &-\sum_{k=1}^{N}(-1)^k\cos\alpha_k = \tfrac{1}{4}\left(2 + (-1)^{N-1}m\pi\right) \\ &-\sum_{k=1}^{N}(-1)^k\cos n\alpha_k = \tfrac{1}{2} \qquad \text{for } n = 5, 7, ..., 3N - \tfrac{3}{2} - \tfrac{1}{2}(-1)^{N-1} \end{aligned} \tag{17.65}$$

where $\alpha_1 < \alpha_2 < ... < \alpha_N < \tfrac{1}{2}\pi\left(1 - \tfrac{1}{6}\left(1 - (-1)^{N-1}\right)\right)$

For *N-1* even, all α_k angles are less than ½π other wise ⅓π (when *N-1* is odd).

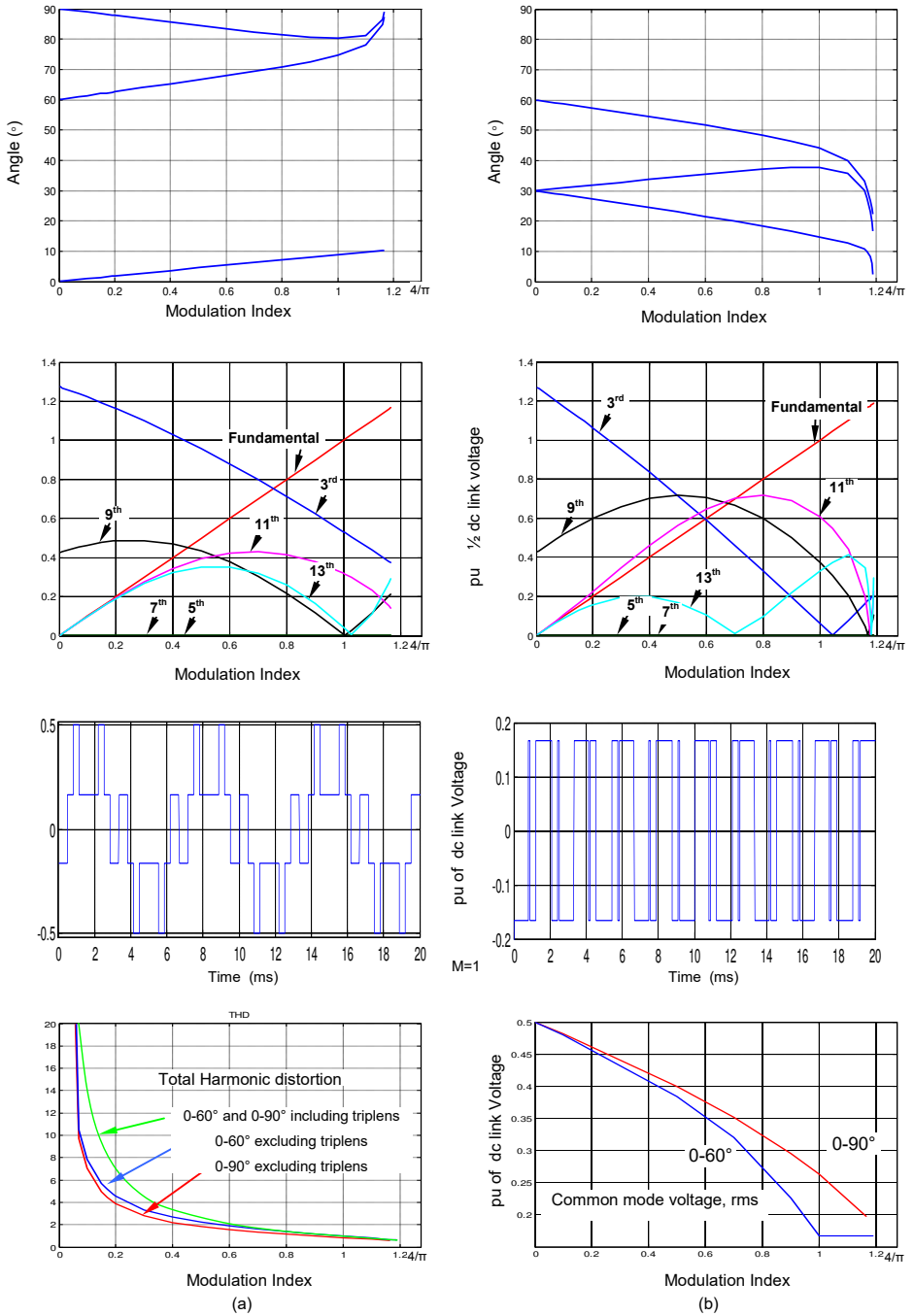


Figure 17.16. *SHE commutation angles, normalised as a function of the fundamental eliminating: the 5th and 7th harmonics with commutation angles (a) 0 to 90° and (b) 0 to 60°.*

To eliminate the 5th and 7th harmonics (an even number of harmonics), with a fundamental magnitude with modulation index *m*, three angles are required, *N*=3 and the three equations to be solved are

$$\cos\alpha_1 - \cos\alpha_2 + \cos\alpha_3 = ¼(2 + m\pi)$$
$$\cos 5\alpha_1 - \cos 5\alpha_2 + \cos 5\alpha_3 = ½$$
$$\cos 7\alpha_1 - \cos 7\alpha_2 + \cos 7\alpha_3 = ½$$

The resultant angles are shown in figure 17.16. The maximum modulation index, with respect to a square wave is 1.166 and 1.188 for angles less that 60 degrees and greater, respectively. Any solution with all angles less than 60° represents dead banding of the three phases, where each phase is alternately clamped to the dc link zero and positive rails (see section 17.1.3vi). The total harmonic distortion is virtually the same in both cases, as is the maximum common mode voltage *dv/dt*, while the rms common mode voltage is greater for the case when the angles can exceed 60 degrees.

To eliminate the 5th, 7th, and 11th harmonics (an odd number of harmonics), with a fundamental magnitude with modulation index *m*, four angles are required, *N*=4 and the four equations to be solved are

$$\cos\alpha_1 - \cos\alpha_2 + \cos\alpha_3 - \cos\alpha_4 = ¼(2 - m\pi)$$
$$\cos 5\alpha_1 - \cos 5\alpha_2 + \cos 5\alpha_3 - \cos 5\alpha_4 = ½$$
$$\cos 7\alpha_1 - \cos 7\alpha_2 + \cos 7\alpha_3 - \cos 7\alpha_4 = ½$$
$$\cos 11\alpha_1 - \cos 11\alpha_2 + \cos 11\alpha_3 - \cos 11\alpha_4 = ½$$

As further harmonics are eliminated, multiple solutions arise, with at least one solution giving a maximum magnitude tending to 1.155 (π/3) in magnitude, compared to 1.27 (4/ π) for a square wave.

17.1.3v - Sinusoidal pulse-width modulation (pwm), SPWM

1 - Natural sampling

(a) Synchronous carrier

The output voltage waveform and method of generation for synchronous carrier, natural sampling sinusoidal pwm, suitable for the single-phase bridge of figure 17.1, are illustrated in figure 17.17. The switching points are determined by the intersection of the triangular carrier wave f_c and the reference modulation sine wave, f_o. The output frequency is at the sine-wave frequency f_o and the output voltage is proportional to the magnitude of the sine wave. The amplitude M ($0 \le M \le 1$) is called the modulation index. For example, figure 17.17a shows maximum voltage output *(M* = 1), while in figure 17.17b where the sine-wave magnitude is halved *(M* = 0.5*),* the output voltage is halved.

If the frequency of the modulation sinewave, f_o, is an integer multiple of the triangular wave carrier-frequency, f_c that is, $f_c = nf_o$ where n is integer, then the modulation is *synchronous,* as shown in figure 17.17. If n is odd then the positive and negative output half cycles are symmetrical and the output voltage contains no even harmonics. In a three-phase system if n is a multiple of 3 (and odd), the carrier is a triplen of the modulating frequency and the spectrum does not contain the carrier or its harmonics.

$$f_c = (6q + 3)\, f_o = nf_o \qquad (17.66)$$

for q = 1, 2, 3.

The Fourier harmonic magnitudes of the line to line voltages are given by

$$a_n = V_f \cos\left(\frac{n\pi}{2}\right)\cos\left(\frac{n\pi}{3}\right)$$
$$b_n = V_f \sin\left(\frac{n\pi}{2}\right)\sin\left(\frac{n\pi}{3}\right) \qquad (17.67)$$

where V_f is proportional to the dc supply voltage V_s and the modulation index M.

Sinusoidal pwm requires a carrier of much higher frequency than the modulation frequency. The generated rectilinear output voltage pulses are modulated such that their duration is proportional to the instantaneous value of the sinusoidal waveform at the centre of the pulse; that is, the pulse area is proportional to the corresponding value of the modulating sine wave.

If the carrier frequency is very high, an averaging effect occurs, resulting in a sinusoidal fundamental output with high-frequency harmonics, but minimal low-frequency harmonics.

Rather than using two offset triangular carriers, as shown in figure 17.17, a triangular carrier without an offset can be used. Now the output only approximates the ideal. Figure 17.18 shows this pwm generation technique and voltage bipolar output waveform, when applied to the three-phase VSI inverter in figure 17.7. Two offset carriers are not applicable to six-switch, three-phase pwm generation since complementary switch action is required. That is, one switch in the inverter leg must always be on.

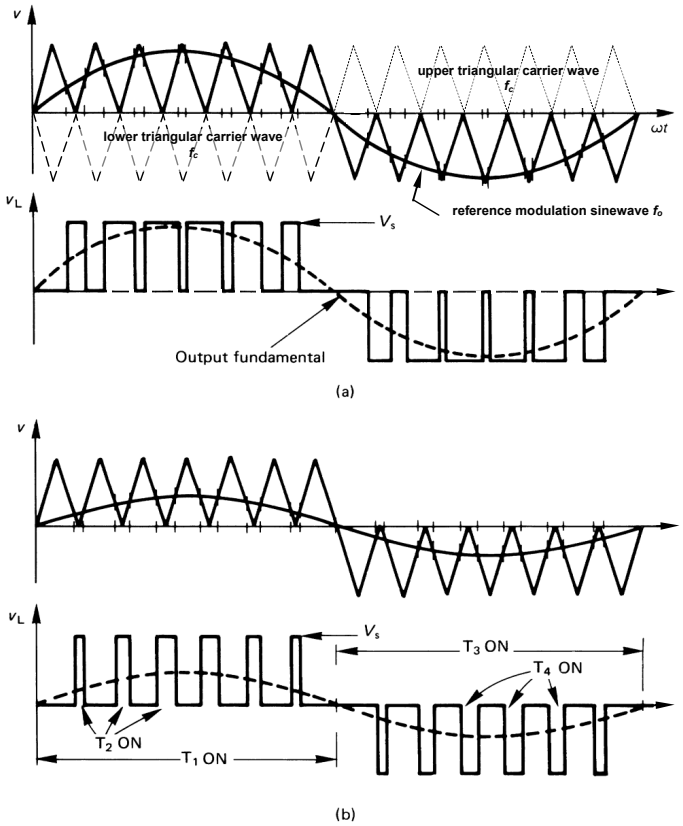


Figure 17.17. *Derivation of trigger signals for multi-level naturally sampled pulse-width modulation waveforms: (a) for a high fundamental output voltage (M = 1) and (b) for a lower output voltage (M = 0.5), with conducting devices shown.*

It will be noticed that, unlike the output in figure 17.17, no zero voltage output periods exist. This has the effect that, in the case of GCT thyristor bridges, a large number of commutation cycles is required. When zero output periods exist, as in figure 17.12, one GCT thyristor is commutated and the complementary device in that leg is not turned on. The previously commutated device can be turned back on without the need to commutate the complementary device, as would be required with the pwm technique illustrated in figure 17.18. Commutation losses are reduced, control circuitry simplified and the likelihood of simultaneous conduction of two series leg devices is reduced.

The alternating zero voltage loop concept can be used, where in figure 17.18b, rather than T_1 being on continuously during the first half of the output cycle, T_2 is turned off leaving T_1 on, then when either T_1 or T_2 must be turned off, T_1 is turned off leaving T_2 on.

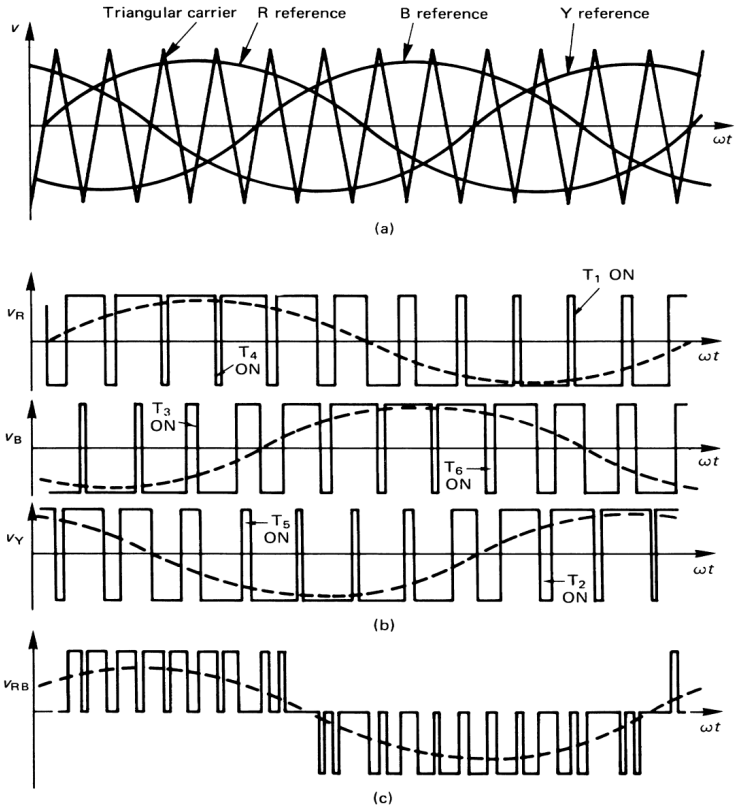


Figure 17.18. *Naturally sampled pulse-width modulation waveforms suitable for a three-phase bridge inverter: (a) reference signals; (b) conducting devices and fundamental sine waves; and (c) one output line-to-line voltage waveform.*

(b) Asynchronous carrier

When the carrier is not an integer multiple of the modulation waveform, asynchronous modulation results. Because the output frequency, f_o, is usually variable over a wide range, it is difficult to ensure $f_c = nf_o$. To achieve synchronism, the carrier frequency must vary with frequency f_o. Simpler generating systems result if a fixed carrier frequency is used, resulting in asynchronism between f_o and f_c at most output frequencies. Left over, incomplete carrier cycles create slowly varying output voltages, called subharmonics, which may be troublesome with low carrier frequencies, as found in high-power drives. Natural sampling, asynchronous sinusoidal pwm is usually restricted to analogue or ASIC implementation. The harmonic consequences of asynchronous-carrier natural-sampling are similar to asynchronous-carrier regular-sampling in 2 to follow.

2 - Regular sampling

(a) Asynchronous carrier

When a fixed carrier frequency is used, usually no attempt is made to synchronise the modulation frequency. The output waveforms do not have quarter-wave symmetry which produces subharmonics. These subharmonics are insignificant if $f_c >> f_o$, usually, $f_c > 20 f_o$.

The implementation of sinusoidal pwm with microprocessors or digital signal processors is common because of flexibility and the elimination of analogue circuitry associated problems. The digital pwm generation process involves scaling, by multiplication, of the per unit sine-wave samples stored in ROM.

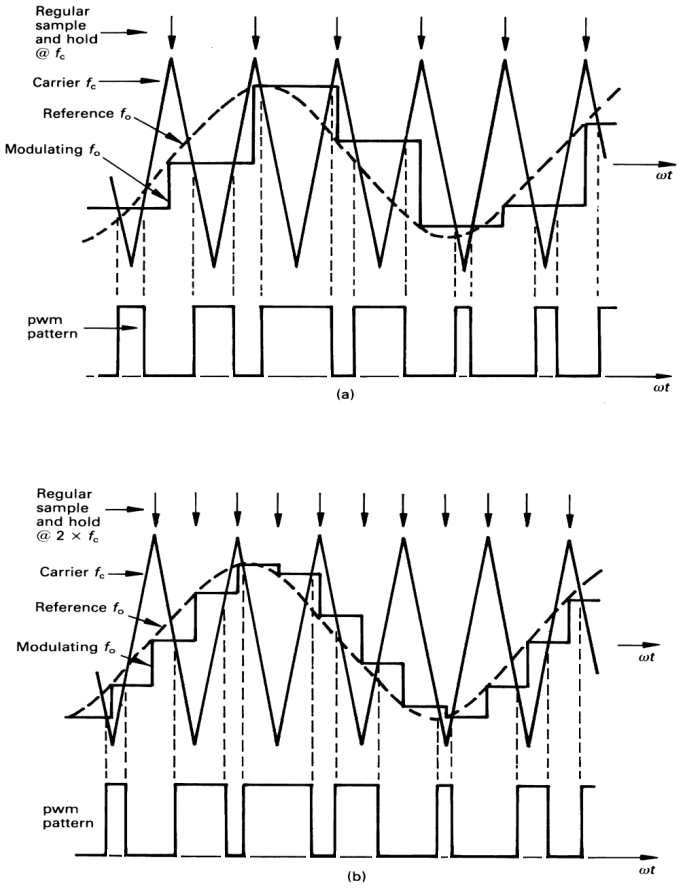


Figure 17.19. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation: (a) symmetrical modulation and (b) asymmetrical modulation.*

The multiplication process is time-consuming, hence natural sampling is not possible. In order to minimise the multiplication rate, the sinusoidal sine-wave reference is replaced by a quantised stepped representation of the sine-wave. Figure 17.19 shows two methods used. Sampling is synchronised to the carrier frequency and the multiplication process is performed at twice the sampling rate for three-phase pwm generation (the third phase can be expressed in terms of two phases, since $v_1 + v_2 + v_3 = 0$).

- *Symmetrical modulation*

Figure 17.19a illustrates the process of symmetrical modulation, where sampling is at the carrier frequency. The quantised sine-wave is stepped and held at each sample point. The triangular carrier is then compared with the step sine-wave sample. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier with the stepped sine-wave, about the non-sampled carrier peak, are equidistant about the carrier peak. The pulse width, independent of the modulation index *M,* is symmetrical about the triangular carrier peak not associated with sampling, as illustrated by the upper pulse in figure 17.20. The pulse width is given by

$$t_{ps} = \frac{1}{2f_c}\left(1 - M \sin 2\pi f_o t_1\right) \qquad (17.68)$$

where t_1 is the time of sampling.

- *Asymmetrical modulation*

Asymmetrical modulation is produced when the carrier is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency, as shown in figure 17.19b. Each side of the triangular carrier about a sampling point intersects the stepped waveform at different step levels. The resultant pulse width is asymmetrical about the sampling point, as illustrated by the lower pulse in figure 17.20 for two modulation waveform magnitudes. The pulse width is given by

$$t_{pa} = \frac{1}{2f_c}\left(1 - \tfrac{1}{2}M\left(\sin 2\pi f_o t_1 + \sin 2\pi f_o t_2\right)\right) \qquad (17.69)$$

where t_1 and t_2 are the times at sampling such that $t_2 = t_1 + 1/2f_c$.

Figure 17.20 shows that a change in the modulation index M varies the pulse width on each edge, termed *double edge modulation*. A triangular carrier produces double edge modulation, while a sawtooth carrier produces *single edge modulation*, independent of the sampling technique.

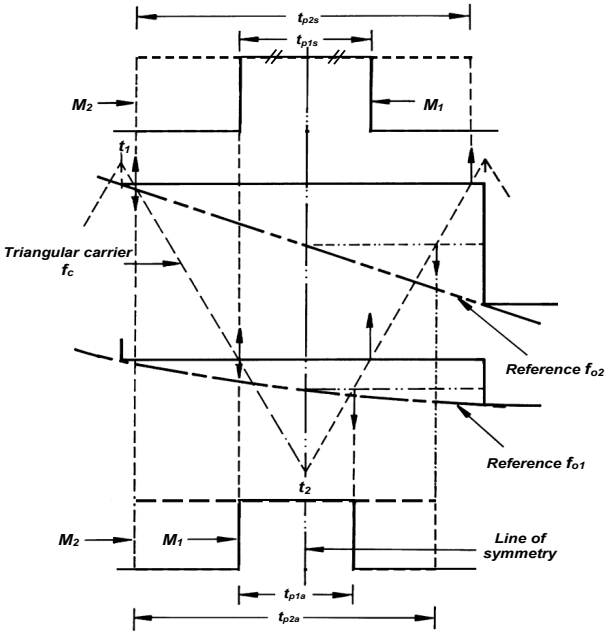


Figure 17.20. *Regular sampling, asynchronous, sinusoidal pulse-width-modulation, showing double edge: (upper) asymmetrical modulation and (lower) symmetrical modulation.*

3 - Frequency spectra of pwm waveforms

The most common form of sinusoidal modulation for three-phase inverters is regular sampling, asynchronous, fixed frequency carrier, pwm. If $f_c > 20f_o$, low frequency subharmonics can be ignored. The output spectra consists of the modulation frequency f_o with magnitude M. Also present are the spectra components associated with the triangular carrier, f_c. For any sampling, these are f_c and the odd harmonics of f_c. (The triangular carrier f_c contains only odd harmonics). These decrease in magnitude with increasing frequency. About the frequency nf_c are components of f_o spaced at $\pm 2f_o$, which generally decrease in magnitude when further away from nf_c. That is, at f_c the harmonics present are f_c, $f_c \pm 2f_o$, $f_c \pm 4f_o$, … while about $2f_c$, the harmonics present are $2f_c \pm f_0$, $2f_c \pm 3f_o$,..., but $2f_c$ is not present. The typical output spectrum is shown in figure 17.21. The relative magnitudes of the sidebands vary with modulation depth and the carrier related frequencies present, f_h, are given by

$$f_h = \tfrac{1}{2}\left(1 + (-1)^{n+1}\right) n f_c \pm \left(2k - \tfrac{1}{2}\left(1 + (-1)^n\right)\right) f_o \qquad (17.70)$$

where $k = 1, 2, 3,....$ (sidebands) and $n = 1, 2, 3,....$ (carrier)

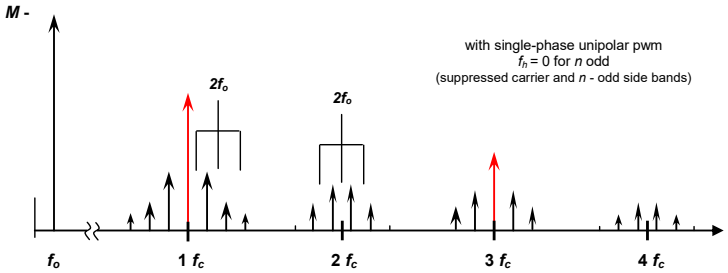
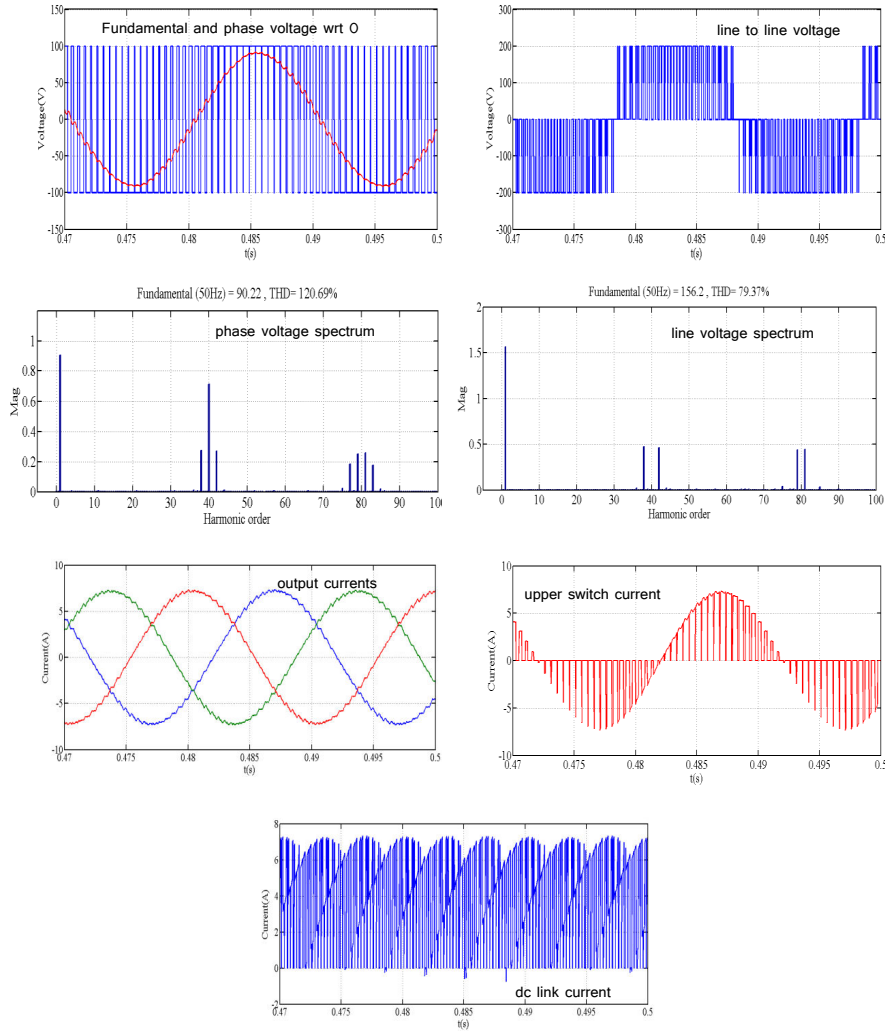


Figure 17.21. *Location of carrier harmonics and modulation frequency sidebands, showing all sideband separated by $2f_m$.*



Waveforms for ideal switch model of the voltage source inverter
(modulation index m=0.9, 2kHz switching frequency, 200V dc link voltage)

Although the various pwm techniques produce other less predominate spectra components, the main difference is seen in the magnitude of the carrier harmonics and sidebands. The magnitudes increase as the pwm type changes from naturally sampling to regular sampling, then from asymmetrical to symmetrical modulation, and finally from double edge to single edge. With a three-phase inverter, the carrier f_c and its harmonics do not appear in the line-to-line voltages since the carrier f_c and in particular its harmonics, are co-phase to the three modulation waveforms.

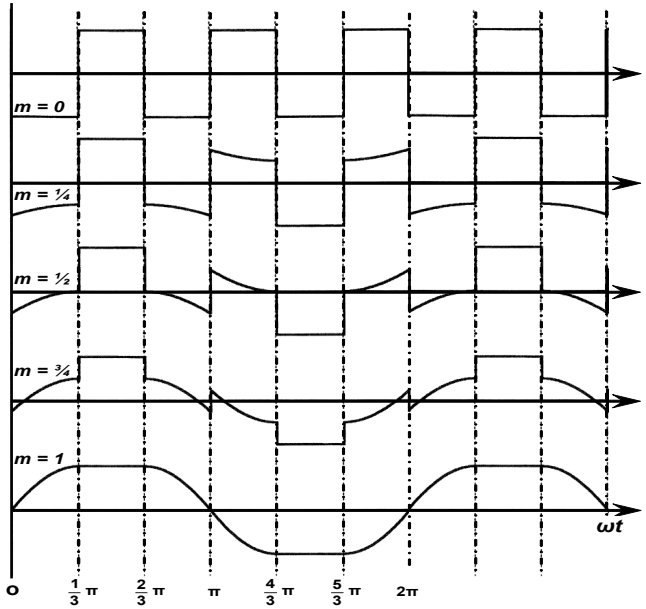


Figure 17.22. *Modulation reference waveform for phase dead banding.*

17.1.3vi - Phase dead-banding, DBPWM

Dead banding is when one phase (leg) is in a fixed on state, and the remaining phases are appropriately modulated so that the phase currents remain sinusoidal. The dead banding occurs for 60° periods of each cycle with the phase with the largest magnitude voltage being permanently turned on. Sequentially each switch is clamped to the appropriate link rail. The leg output is in a high state if it is associated with the largest positive phase voltage magnitude, while the phase output is zero if it is associated with the largest negative phase magnitude. Thus the phase outputs are cycled, being alternately clamped high and low for 60° every 180° as shown in figure 17.22. A consequence of dead banding is reduced switching losses since each leg is not switched at the carrier frequency for 120° (two 60° periods 180° apart). A consequence of dead banding is increased ripple current. Dead banding is achieved with discontinuous modulating reference signals. Dead banding for a continuous 120° per phase leg is also possible but the switching loss savings are not uniformly distributed amongst the six inverter switches.

The magnitude of the fundamental (with respect to the ac mains) when using standard PWM can be increased by 2/√3 from 3x√3/2π, 0.827pu to 3/π, 0.955pu without introducing output voltage distortion, by the injection of triplen components, which are co-phasal in a three-phase system, and therefore do not appear in the line currents. Two approaches can be used to affect this undistorted output voltage magnitude increase.

- Triplen injection into the modulation waveform or
- Voltage space vector modulation

17.1.3vii - Triplen Injection modulation

1 - Triplens injected into the modulation waveform, THI

An inverter reconstitutes three-phase voltages with a maximum magnitude of 0.827 ($3\sqrt{3}/2\pi$) of the fixed three-phase input ac supply, converted to dc before inversion. A motor designed for the fixed mains supply is therefore under-fluxed at rated frequency and not fully utilised on an inverter. As will be shown, by using third harmonic voltage injection, the flux level can be increased to 0.955 ($3/\pi$) of that produced on the three-phase ac mains supply.
If over-modulation *(M* > 1) is not allowed, then the modulation wave $M \sin \omega t$ is restricted in magnitude to $M = 1$, as shown in figure 17.23a.

If $V_{RN} = M \sin\omega t \le 1$pu
and $V_{YN} = M \sin(\omega t + \frac{2}{3}\pi) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M \sin(\omega t - \frac{1}{6}\pi)$
where $0 \le M \le 1$

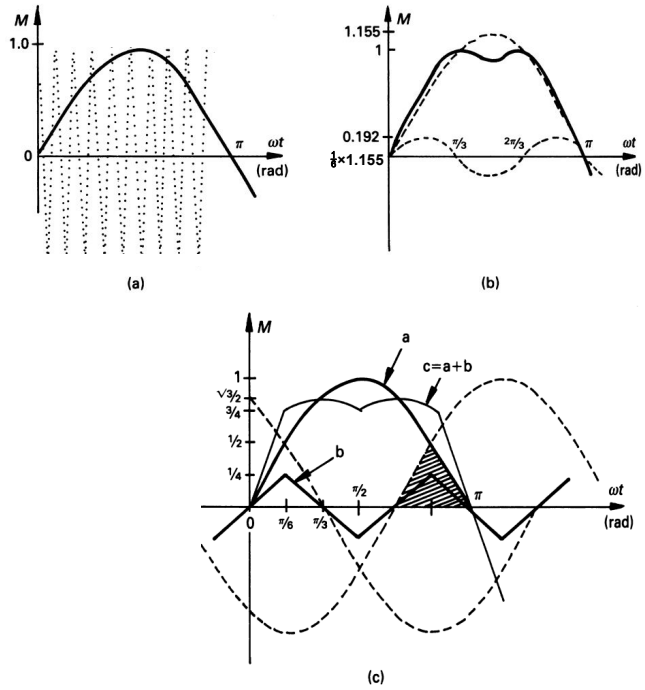


Figure 17.23. *Modulation reference waveforms: (a) sinusoidal reference, sin ωt; (b) third harmonic injection reference, sin ωt + $\frac{1}{6}$sin 3ωt; and (c) triplen injection reference, sin ωt + (1/√3n){9/8 sin3ωt - 80/81 sin9ωt + . ..} where the near triangular waveform b is half the magnitude of the shaded area.*

In a three-phase pwm generator, the fact that harmonics at $3f_o$ (and odd multiplies of $3f_o$) vectorally cancel can be utilised effectively to increase *M* beyond 1, yet still ensure modulation occurs for every carrier frequency cycle.

Let $V_{RN} = M' \sin\omega t + \frac{1}{6} \sin 3\omega t) \le 1$ pu
and $V_{YN} = M' (\sin(\omega t + \frac{2}{3}\pi) + \frac{1}{6} \sin 3(\omega t + \frac{2}{3}\pi)) \le 1$ pu
then $V_{RY} = \sqrt{3}\, M' \sin(\omega t - \frac{1}{6}\pi)$

V_{RN} has a maximum instantaneous value of 1 pu at $\omega t = \pm\frac{1}{3}\pi$, as shown in figure 17.23b. Therefore

$$V_{RN}\left(\omega t = \tfrac{1}{3}\pi\right) = \frac{\sqrt{3}}{2} M' = 1$$

that is

$$\widehat{M}' = \frac{2}{\sqrt{3}}\widehat{M} = 1.155\widehat{M} \tag{17.71}$$

Thus the fundamental of the phase voltage is M' sin ωt = 1.155 M sin ωt. That is, if the modulation reference sin ωt + $\frac{1}{6}$ sin $3\omega t$ is used, the fundamental output voltage is 15.5 per cent larger than when sin ωt is used as a reference. The increased fundamental is shown in figure 17.23b.

The spatial voltage vector technique injects the triplens according to

$$V_{RN} = M'\left\{\sin\omega t + \frac{1}{\sqrt{3}\pi}\sum_{r=0}^{\infty}\frac{-1^{r}}{\left[(2r+1)-\frac{1}{3}\right]\left[(2r+1)+\frac{1}{3}\right]}\sin\left[(2r+1)3\omega t\right]\right\} \tag{17.72}$$

The Fourier triplen series represents half the magnitude of the shaded area in figure 17.23c (the waveform marked 'b'), which is formed by the three-phase sinusoidal waveforms. The spatial voltage vector waveform is defined by

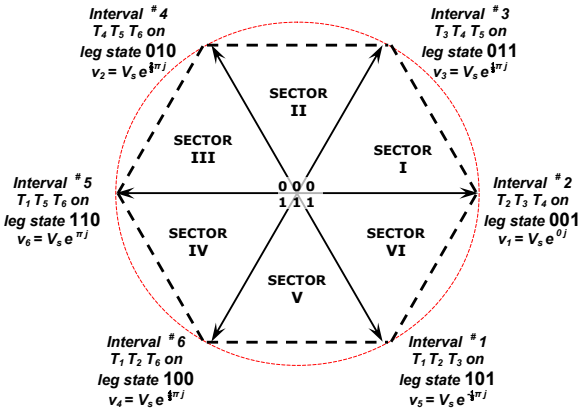
$$\begin{aligned} &\frac{3}{2}\sin\omega t && 0 \le \omega t \le \tfrac{1}{6}\pi \\ &\frac{\sqrt{3}}{2}\sin(\omega t + \tfrac{1}{6}\pi) && \tfrac{1}{6}\pi \le \omega t \le \tfrac{1}{2}\pi \end{aligned} \tag{17.73}$$

The use of this reference increases the duration of the zero volt loops, thereby decreasing inverter output current ripple. The maximum modulation index is 2/√3, 1.155. Third harmonic injection, yielding M = 1.155, is a satisfactory approximation to spatial voltage vector injection.

2 - Voltage space vector pwm, SVM

When generating three-phase quasi-square output voltages, the inverter switches step progressively to each of the six switch output possibilities (states). In figure 17.10, when producing the quasi-square output, each of these six states is represented by an output voltage space vector. Each vector has a ⅓π displacement from its two adjacent states, and each has a length V_s which is the pole output voltage relative to the inverter 0V rail. Effectively, the quasi-square three-phase output is generated by a rotating vector of length V_s, jumping successively from one output state to the next in the sequence, and in so doing creating six voltage output sectors. The speed of rotation, in particular the time for one rotation, determines the inverter output frequency. The sequence of voltage vectors {v_1, v_3, v_2, v_6, v_4, v_5} is arranged such that stepping from one state to the next involves only one of the three poles changing state. Thus the number of inverter devices needing to change states (switch) at each transition, is minimised. But multiple steps occur if the carrier frequency is not a six times multiple of the fundamental frequency.

[If the inverter switches are relabelled, upper switches T_1, T_2, T_3 - right to left; and lower switches T_4, T_5, T_6 - right to left: then the rotating voltage sequence becomes {v_1, v_2, v_3, v_4, v_5, v_6}]



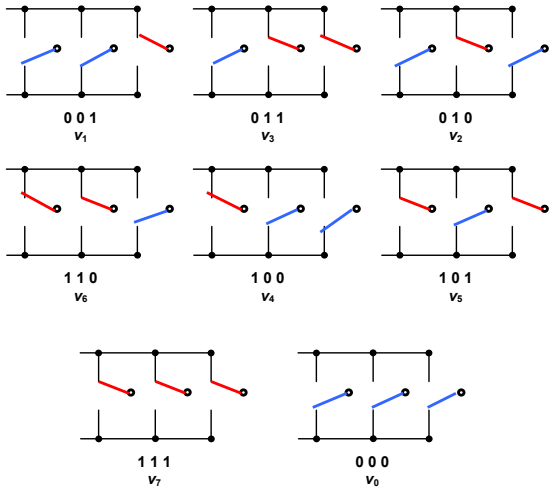


Figure 17.24. *Instantaneous output voltage states for the three legs of an inverter.*

Rather than stepping ⅓π radians per step, from one voltage space vector position to the next, thereby producing a six-step quasi-square fixed magnitude voltage output, the rotating vector is rotated in smaller steps based on the position being updated at a constant rate (carrier frequency). Furthermore, the vector length can be varied, modulated, to a magnitude less than V_s.

$$\begin{aligned} \frac{t_a}{T_c} &= \frac{|V_a|}{|V_1|} = \frac{\frac{2}{\sqrt{3}}V_{o/p}\sin\left(\frac{1}{3}\pi - \theta\right)}{V_s} \\ \frac{t_b}{T_c} &= \frac{|V_b|}{|V_3|} = \frac{\frac{2}{\sqrt{3}}V_{o/p}\sin\theta}{V_s} \qquad \text{where } |V_1| = |V_3| \end{aligned} \tag{17.74}$$

To incorporate a variable length rotating **vector length** (modulation depth), it is necessary to vary the average voltage in each carrier period. Hence pulse width modulation is used in the period between each finite step of the rotating vector. Pulse width modulation requires the introduction of zero voltage output states, namely all the top switches on (state 111, v_7) or all the lower switches on (state 000, v_0). These two extra states are shown in figure 17.24, at the centre of the hexagon. Now the pole-to-pole output voltage can be zero, which allows duty cycle variation to achieve variable average output voltage for each phase, within each carrier period, proportional to the magnitude of the position vector.
To facilitate **vector positions** (angles) that do not lie on one of the six quasi-square output vectors, an intermediate vector $V_{o/p}\,e^{j\theta}$ is resolved into the vector sum of the two quasi-square vectors adjacent to the rotating vector. This process is shown in figure 17.25 for a voltage vector $V_{o/p}$ that lies in sector I, between output states v_1 (001) and v_3 (011). The voltage vector has been resolved (using Park's transformation) into the two components V_a and V_b as shown.

The time represented by quasi-square vectors v_1 and v_3 is the carrier period T_c, in each case. Therefore the portion of T_c associated with v_a and v_b is scaled proportionally to v_1 and v_3, giving t_a and t_b.

The two sine terms in equation (17.74) generate two sine waves displaced by 120°, identical to that generated with standard carrier based sinusoidal pwm.
The sum of t_a and t_b cannot be greater than the carrier period T_c, thus

$$\begin{aligned} t_a + t_b &\le T_c \\ t_a + t_b + t_o &= T_c \end{aligned} \tag{17.75}$$

where the slack variable t_o has been included to form an equality. The equality dictates that vector v_1 is used for a period t_a, v_3 is used for a period t_b, and during period t_o, the null vector, v_0 or v_7, at the centre of the hexagon is used, which do not affect the average voltage during the carrier interval T_c.

A further constraint is imposed in the time domain. The rotating voltage vector is a fixed length for all rotating angles, for a given inverter output voltage. Its length is restricted in both time and space. Obviously the resolved component lengths cannot exceed the pole vector length, V_s. Additionally, the two vector magnitudes are each a portion of the carrier period, where t_a and t_b could be both equal to T_c, that is, they both have a maximum length V_s. The anomaly is that voltages v_a and v_b are added vectorially but their scalar durations (times t_a and t_b) are added linearly. The longest time $t_a + t_b$ possible is when t_o is zero, as shown in figures 17.25a and 17.24a, by the hexagon boundary. The shortest vector to the boundary is where both resolving vectors have a length ½V_s, as shown in figure 17.25b. For such a condition, $t_a = t_b = ½T_c$, that is $t_a + t_b = T_c$. Thus for a constant inverter output voltage, when the rotating voltage vector has a constant length, $\hat{V}_{o/p}$ the locus of allowable rotating reference voltage vectors must be within the circle scribed by the maximum length vector shown in figure 17.25b. As shown, this vector has a length $v_1 \cos 30°$, specifically $0.866V_s$. Thus the full quasi-square vectors v_1, v_2, etc., which have a magnitude of $1 \times V_s$, cannot be used for generating a sinusoidal output voltage. The excess length of each quasi-square voltage (which represents time) is accounted for by using zero state voltage vectors for a period corresponding to that extra length (1- cos30° at maximum output voltage).
The dwell time calculations for all six sectors are

$$\begin{aligned} t_a &= \tfrac{\sqrt{3}}{2} m T_c \sin(\tfrac{1}{3} n\pi - \theta) \\ t_b &= \tfrac{\sqrt{3}}{2} m T_c \sin(\theta - \tfrac{1}{3}(n-1)\pi) \\ t_o &= T_c - t_a - t_b \end{aligned} \qquad (17.76)$$

where n represents sector number, 1 to 6, and m is modulation index $m = V_{o/p} / V_s$.
Having calculated the necessary periods for the inverter poles (t_a, t_b, and t_o), the carrier period switching pattern can be assigned in two ways.

- Minimised current ripple
- Minimised switching losses, using dead banding

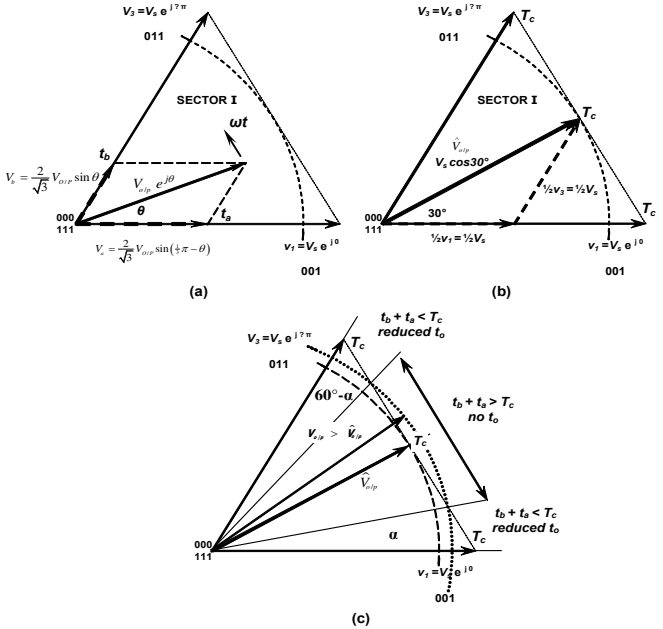


Figure 17.25. *First sector of inverter operational area involving pole outputs 001 and 011: (a) general rotating voltage vector; (b) maximum allowable voltage vector length for undistorted output voltages; and (c) over modulation.*

Each approach is shown in figure 17.26, using single edged modulation. The waveforms are based on the equivalent of symmetrical modulation where the pulses are symmetrical about the carrier trough. By minimising the current ripple, seven switch states are used per carrier cycle, while for loss minimisation (dead banding) only five switch states occur, but at the expense of increased ripple current in the output

current. When dead banding, the zero voltage state v_0 is used in even numbered sextants and v_7 is used in odd numbered sextants.
Sideband and harmonic component magnitudes can be decreased if double-edged modulation placement of the states is used, which requires recalculation of t_a, t_b, and t_o at the carrier crest, as well as at the trough.

Over-modulation is when the magnitude of the demanded rotating vector is greater than $\hat{V}_{o/p}$ such that the zero voltage time reduces to zero, $t_o = 0$, during a portion of the time of one rotation of the output vector. Initially this occurs at 30° $\left(\frac{1}{6}\pi(2N_{\text{sector}} - 1)\right)$ when the output vector length reaches $\hat{V}_{o/p}$, as shown in figure 17.25b. As the demand voltage magnitude increases further, the region around the 30° vector position where t_o ceases to occur, increases as shown in figure 17.25c. When the output rotational vector magnitude increases to V_s, the maximum possible, angle α reduces to zero, and t_o ceases to occur at any rotational angle. The values of t_a, t_b, and t_o (if greater than zero), are calculated as usual, but pulse times are assigned pro rata to fit within the carrier period T_c.

The switching frequency can be decreased by using dc-link clamping like in 17.1.3vi. Each leg is successively clamped, alternately to each dc rail (that is states 000 and 111 are alternated every 60° when a zero state is required). For example, in sector 1, an odd sector number, the sequence would be states [111] [011] [001] [011] [111]. In sector 2, an even sector number, the sequence would be states [000] [010] [001] [010] [000]. In odd sector number zero vector [111] is used, while [000] is used in even numbered sector.

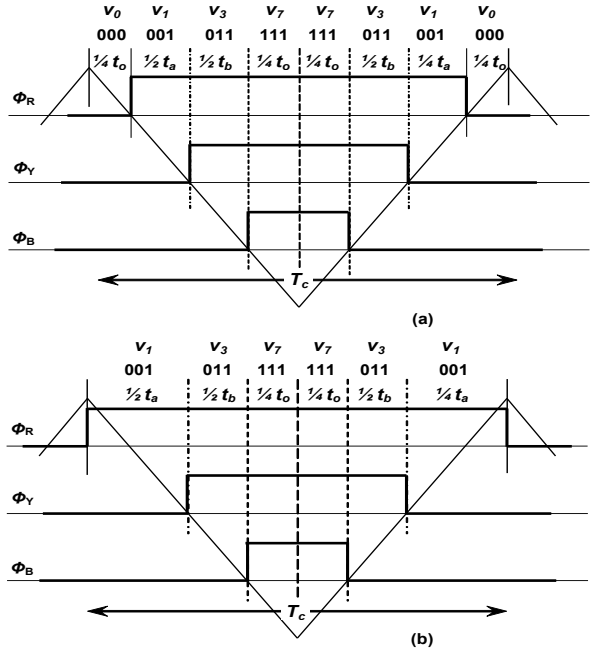


Figure 17.26. *Assignment of pole periods t_a and t_b based on: (a) minimum current ripple and (b) minimum switching transitions per carrier cycle, T_c.*

17.1.4 Assessment of PWM modulation techniques

The following are some considerations when comparing different modulation techniques:

- Good utilization of DC power supply, that is, to deliver high output voltage for a given DC supply
- Good linearity in voltage and or current control
- Low harmonic content in the output voltage and currents, especially in the low-frequency region
- Low switching losses

Figure 17.27 compares different PWM modulating signals, namely SPWM, THI, DBPWM and SVM, for a three-phase inverter with a 500Hz switching frequency via a triangular carrier signal. Figure 17.27a shows the fundamental inverter output phase voltage at different modulation indices where THI, DBPWM and SVM give a higher fundamental component than SPWM. Figure 17.27b shows inverter output phase voltage THD at different modulation indices where SPWM gives the highest THD. Distortion factor, DF for inverter output phase voltage at different modulation indexes in Figure 17.27c shows that THI gives the lowest DF at higher modulation indices.

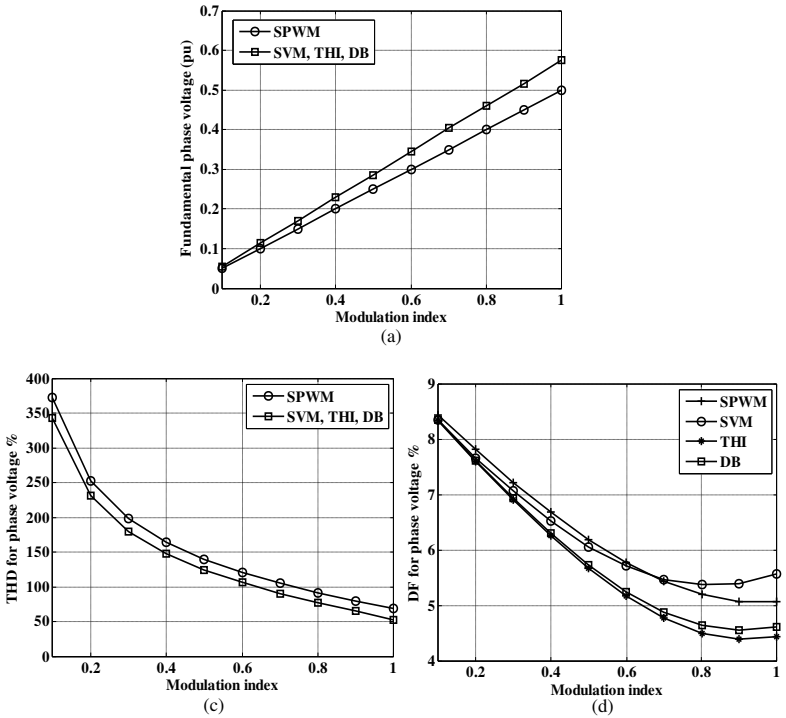


Figure 17.27. *Performance parameters for different modulation techniques: (a) fundamental phase voltage; (b) THD for the phase voltage; and (c) DF for the phase voltage.*

17.1.5 Common mode voltage

The common mode CM voltage is a remanent voltage with respect to a reference zero 'o' as shown in figure 17.28(a). The line voltages and a common mode voltage V_{cm} can be derived based on leg phase voltages (V_{ao}, V_{bo}, V_{co}) of a two-level three-phase inverter, as follows:

$$V_{ao} = V_{an} + V_{cm}$$
$$V_{bo} = V_{bn} + V_{cm}$$
$$V_{co} = V_{cn} + V_{cm}$$

The sum of the leg voltages is given by :

$$V_{ao} + V_{bo} + V_{co} = (V_{an} + V_{bn} + V_{cn}) + 3V_{cm}$$

In a three-phase system:

$$V_{an} + V_{bn} + V_{cn} = 0$$

thus the common mode voltage source in a three-phase system is:

$$V_{cm}(t) = \tfrac{1}{3}\left(V_{ao}(t) + V_{bo}(t) + V_{co}(t)\right) = \tfrac{1}{3}\left(V_a(t) + V_b(t) + V_c(t)\right)$$

where V_a, V_b, V_c are the phase voltages, n is the load neutral, and o is the split dc link centre voltage node.

The CM voltage is a staircase function with steps of $\frac{1}{3}V_{dc}$ (V_{dc} - dc link voltage) within a frequency of three time the inverter modulation frequency, plus carrier related modulation steps superimposed, as shown in figure 17.28. Because the Kirchhoff voltage loop is usually completed by capacitance, a train of damped sinewave pulses of CM current flows as a result of each CM voltage step. In electrical machines such currents cause bearing deterioration. Generally, in electrical circuits, the CM currents through substrates, isolation capacitance, etc., produce and inject electrical noise and cause EMC interference.

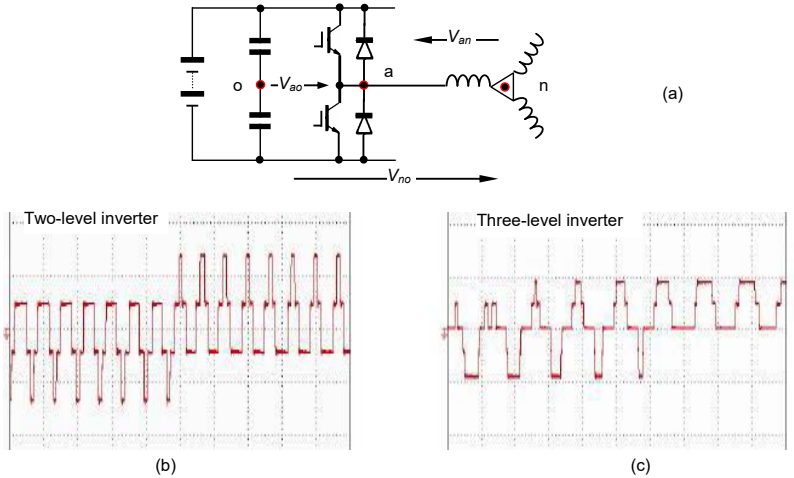


Figure 17.28. *Inverter common mode voltage: (a) source voltages, (b) two level inverter common mode voltage, and (c) three level inverter common mode voltage.*

17.1.6 DC link voltage boosting

Both triplen injection and SVM under flux a 50/60Hz machine designed to operate from a given three-phase ac mains supply. Increased dc rail voltage (over that produced from rectification) can be achieved with the three-phase boost converter shown in figure 17.29. Additionally, being a boost converter, the ac input current can be continuous, and forced to track any reference whilst maintaining the transferred power balance between the input and the output. By using the ac mains as references, the input current can be sinusoidal, of high quality and at any desired angle, usually in phase with the supply voltage - unity power factor. The bridge acts as an uncontrolled rectifier when the output voltage is below the mains rectified level, as during start-up when the dc link capacitor is uncharged. Near instantaneous power reversal (by current direction reversal) is possible when the converter acts as a dc to ac inverter. The power factor angle and three-phase voltage magnitude can be varied to control the active and reactive power flows back into the ac grid. PWM or SVM control can insure sinusoidal current in both conversion directions. Unbeknown to the power electronics community, this so called 'boost' converter can control the dc output down to 0.86 the uncontrolled rectifier level if third harmonics (or SVM) are used. As a bidirectional SVM converter (triplen injection), it offers better dc link utilisation as a dc to ac inverter, and better ac source utilisation as an ac to dc converter.

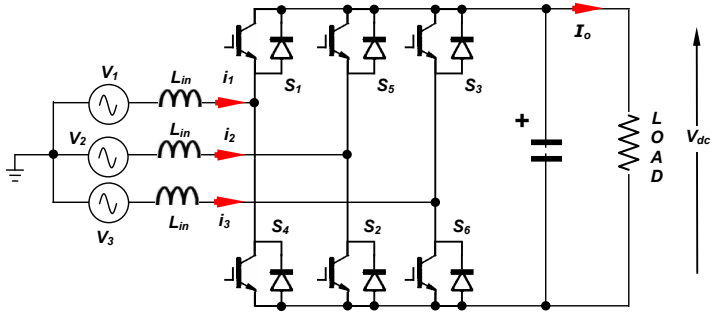


Figure 17.29. *PWM boost three-phase rectifier.*

17.2 DC-to-ac controlled current-source inverters

In the current source inverter, *CSI*, the dc supply is of high reactance, being inductive so as to maintain the required inverter output bidirectional current independent of the inverter load. At medium and low power levels *CSIs* use self commutating devices, as shown in figure 17.30. If IGBTs are used, figure 17.30a, series diodes are need for the necessary reverse blocking requirements, while the GGT devices in 17.30b require symmetrical voltage blocking characteristics.

At high power levels (hvdc), it is still not uncommon to utilise the robustness of thyristor technology that requires external commutation circuitry.

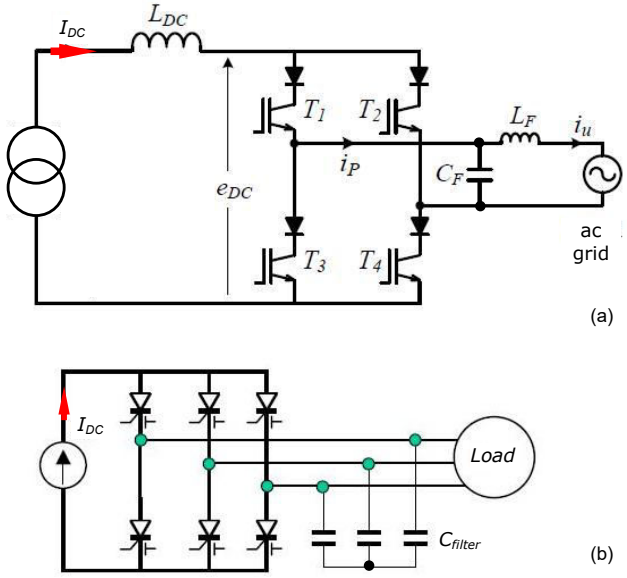


Figure 17.30. *Current source converters: (a) singe phase and (b) three phase.*

17.2.1 Single-phase current source inverter

A single-phase, controlled current-sourced bridge is shown in figure 17.31a and its near square-wave output current is shown in figure 17.31b. No freewheel diodes are required and the thyristors require forced commutation and have to withstand reverse voltages. An inverter current path must be maintained at all times for the source controlled current.
Consider thyristors T_1 and T_2 on and conducting the constant load current. The capacitors are charged with plates X and Y positive as a result of the previous commutation cycle.

- ***Phase I***

Thyristors T_1 and T_2 are commutated by triggering thyristors T_3 and T_4. The capacitors impress negative voltages across the respective thyristors to be commutated off, as shown in figure 17.32a. The load current is displaced from T_1 and T_2 via the path T_3-C_1-D_1, the load and D_2-C_2-T_4. The two capacitors discharge in series with the load, each capacitor reverse biasing the thyristor to be commutated, T_1 and T_2 as well as diodes D_3 to D_4. The capacitors discharge linearly (due to the constant current source).

- ***Phase II***

When both capacitors are discharged, the load current transfers from D_1 to D_2 and from D_3 to D_4, which connects the capacitors in parallel with the load via diodes D_1 to D_2. The plates X and Y now charge negative, ready for the next commutation cycle, as shown in figure 17.32b. Thyristors T_1 and T_2 are now forward biased and must have attained forward blocking ability before the start of phase 2.

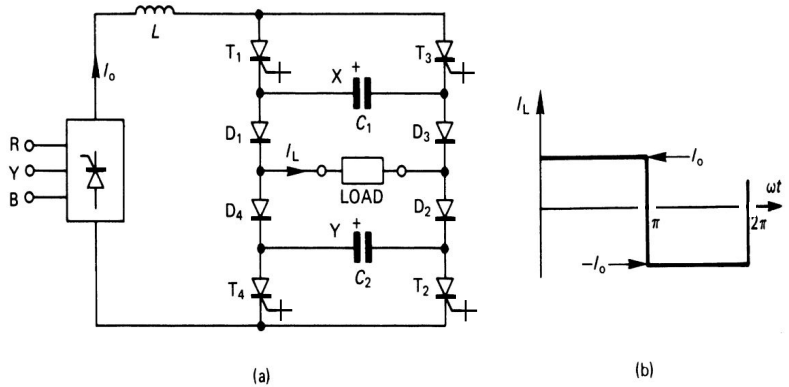


Figure 17.31. *Single-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform.*

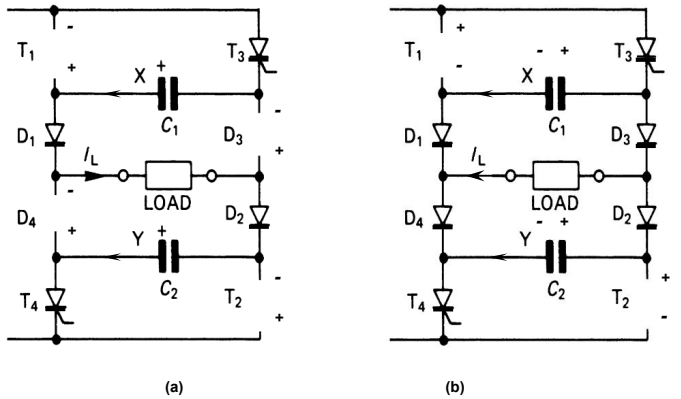


Figure 17.32. *Controlled-current sourced bridge inverter showing commutation of T_1 and T_2 by T_3 and T_4: (a) capacitors C_1 and C_2 discharging and T_1, T_2, D_3, and D_4 reversed biased and (b) C_1, C_2, and the load in parallel with C_1 and C_2 charging.*

The on-going thyristor automatically commutates the outgoing thyristor. This repeated commutation sequencing is a processed termed *auto-sequential thyristor commutation*. The load voltage is load dependent and usually has controlled voltage spikes during commutation.
Since the GTO and GCT both can be commutated from the gate, the two commutation capacitors C_1 and C_2 are not necessary. Commutation overlap is still essential. Also, if the thyristors have reverse blocking capability, the four diodes D_1 to D_4 are not necessary. IGBTs require series blocking diodes, which increases on-state losses. In practice, the current source inverter is only used in very high-power applications (>1MVA), and the ratings of the self-commutating thyristor devices can be greatly extended if the simple external capacitive commutation circuits shown in figure 17.31 are used to reduce thyristor turn-off stresses.

17.2.2 Three-phase current source inverter

A three-phase controlled current-source inverter is shown in figure 17.33a. Only two thyristors can be on at any instant, that is, the 120° thyristor conduction principle shown in figure 17.12 is used. A quasi-square line current results, as illustrated in figure 17.33b. There is a 60° phase displacement between commutation of an upper device followed by commutation of a lower device. An upper device (T_1, T_3, T_5) is turned on to commutate another upper device, and a lower device (T_2, T_4, T_6) commutates another lower device. The three upper capacitors are all involved with each upper device commutation, whilst the same constraint applies to the lower capacitors. Thyristor commutation occurs in two distinct phases.

- ***Phase I***
  In figure 17.34a the capacitors C_{13}, C_{35}, C_{51} are charged with the shown polarities as a result of the earlier commutation of T_5. T_1 is commutated by turning on T_3. During commutation, the capacitor between the two commutating switches is in parallel with the two remaining capacitors which are effectively connected in series. Capacitor C_{13} provides displacement current whilst in parallel, C_{35} and C_{151} in series also provide thyristor T_1 displacement current, thereby reverse biasing T_1.

- ***Phase II***
  When the capacitors have discharged, T_1 becomes forward biased, as shown in figure 17.34b, and must have regained forward blocking capability before the applied positive *dv/dt*. The capacitor voltages reverse as shown in figure 17.34b and when fully charged, diode D_1 ceases to conduct. Independent of this commutation, lower thyristor T_2 is commutated by turning on T_4, 60° later.

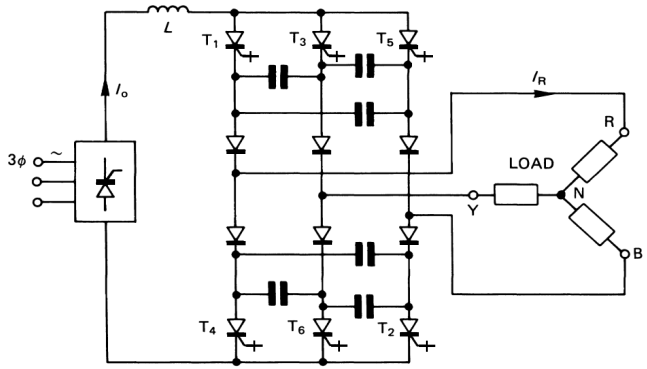


Figure 17.33. *Three-phase controlled-current sourced bridge inverter: (a) bridge circuit with a current source input and (b) load current waveform for one phase showing 120° conduction.*

As with the single-phase current sourced inverter, assisted capacitor commutation can greatly improve the capabilities of self-commutating thyristors, such as the GTO thyristor and GCT. Transient voltage sharing of series connected devices is also aided. The output capacitors stiffen the output ac voltage.

A typical application for a three-phase current-sourced inverter would be to feed and control a three-phase induction motor. Varying load requirements are met by changing the source current level over a number of cycles by varying the link inductor input voltage.
An important advantage of the controlled current source concept, as opposed to the constant voltage link, is good fault tolerance and protection. An output short circuit or simultaneous conduction in an inverter leg is controlled by the current source. Its time constant is usually longer than that of the input converter, hence converter shut-down can be initiated before the link current can rise to a catastrophic level. Stray inductance in the capacitor commutation paths is a major problem at high power levels.

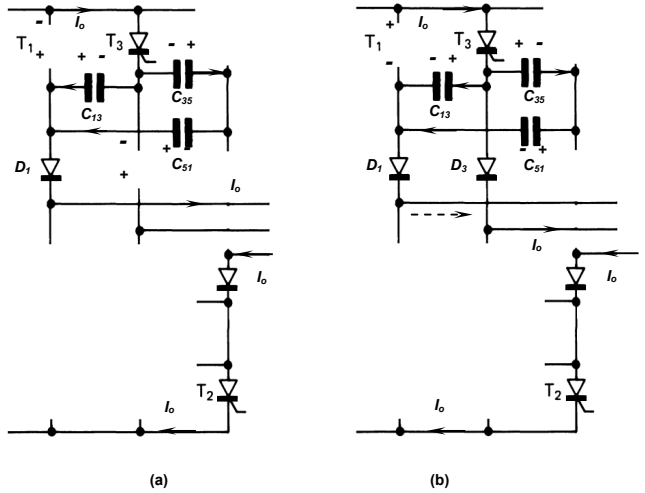


Figure 17.34. *Controlled-current sourced bridge three-phase inverter showing commutation of T_1 and T_3: (a) capacitors C_{13} discharging in parallel with C_{35} and C_{51} discharging in series, with T_1 and D_3 reversed biased (b) C_{13}, C_{35}, and C_{51} charging in series with the load , with T_1 forward biased.*

PWM techniques are applicable to current source inverters in order to reduce current harmonics, thereby reducing load losses and pulsating motor shaft torques. Since current source inverters are most attractive in very high-power applications, inverter switching is minimised by using optimal pwm (selected harmonic elimination). The central 60° portion about the maximums of each phase cannot be modulated, since link current must flow and during such periods both the other phases require the opposite current direction. Attempts to over come such pwm restrictions include using a current sourced inverter with additional parallel current displacement paths as shown in figure 17.35. The auxiliary thyristors, T_{upper} and T_{lower}, and capacitors, C_R, C_Y, and C_B, provide alternative current paths (extra control states) and temporary energy storage. The auxiliary thyristor can be commutated by the extra capacitors. The problem can be alleviated by triplen injection or SVM, which minimises the duration of any such periods in the central 60° blocks, so that the link can be shorted for the short periods.
Characteristics and features of current source inverters

- The inverter is simple and can utilise rectifier grade thyristors. The switching devices must have reverse blocking capability and experience high voltages (both forward and reverse) during commutation. Extra losses are associated with two series devices, a diode and a thyristor.
- Commutation capability is load current dependent and a minimum load is required. This limits the operating frequency and precludes use in UPS systems. The limited operating frequency can result in torque pulsations.
- The inverter can recover from an output short circuit hence the system is rugged and reliable – fault tolerant.
- The converter-inverter configuration has inherent four quadrant capability without extra power components. Power inversion is achieved by reversing the converter average voltage output with a delay angle of $\alpha > \frac{1}{2}\pi$, as in the three-phase fully controlled converter shown in figure 14.11 (or 17.4.3). In the event of a power supply failure, mechanical braking is necessary. Dynamic braking is possible with voltage source systems.
- Current source inverter systems have sluggish performance and stability problems on light loads and at high frequency. On the other hand, voltage source systems have minimal stability problems and can operate open loop.
- Each machine must have its own controlled rectifier and inverter. The dc link of the voltage source scheme can be used by many inverters or many machines can utilise one inverter. A dc link offers limited ride-through.
- Current feed inverters tend to be larger in size and weight, because of the link inductor and filtering requirements.

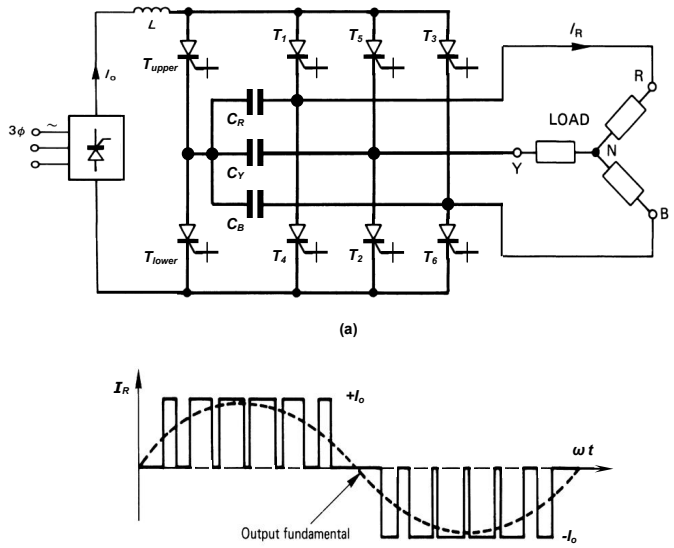


Figure 17.35. *Three-phase controlled-current sourced bridge inverter with alternative commutation current paths: (a) bridge circuit with a current source input and two extra thyristors and (b) load current waveform for one phase showing 180° conduction involving pwm switching.*

17.3 Multi-level voltage-source inverters

The conventional three-phase, six-switch dc to ac voltage-source inverter is shown in figure 17.7. Each of the three inverter legs has an output which can provide one of two voltage levels, V_s, when the upper switch (or diode) is on, and 0 when the lower switch (or diode) conducts. The quality of the output waveform is determined by the resolution and switching frequency of the pwm technique used.

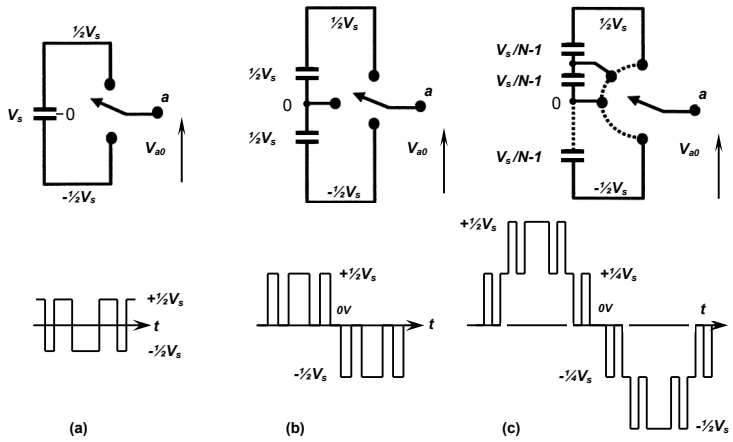


Figure 17.36. *One phase leg of a voltage-source bridge inverter with: (a) two levels; (b) three levels; and (c) N-levels, with N-1 capacitors and waveform for five levels.*

A multilevel inverter (directly or indirectly) divides the dc rail, so that the output of the leg can be more than two discrete levels, as shown in figure 17.36 for a diode clamped multilevel inverter model. In this way, the output quality is improved because both pulse width modulation and amplitude modulation can be used. The output pole is made from more than two series connected, clamped switches, so the total dc voltage rail can be the sum of the voltage rating of the individual switches. Very high output voltages can be achieved, where each device does not experience a voltage in excess of its individual rating.

A multilevel inverter allows higher output voltages with low distortion (due to the use of both pulse width and amplitude modulation) and reduced output *dv/dt*.
There are four main types of multilevel converters

- Diode clamped
- Flying capacitor
- Cascaded H-bridge, and
- Modular multilevel

17.3.1 Diode clamped multilevel inverter

Figure 17.36 shows the basic principle of the diode clamped (or neutral point clamped, NPC) multilevel inverter, where only one dc supply, V_s, is used and N is the number levels present in the output voltage between the leg output and the inverter negative terminal, $V_{a\text{-}neg}$. The capacitors split the dc rail voltage into a number of lower voltage levels, each of which can be tapped and connected to the leg output through switches (and diodes). Only one string of series connected capacitors is necessary for any number of output phase legs.
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{17.77}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{17.78}$$

The number of capacitors required, independent of the number of phase, is

$$N_{cap} = N - 1 \tag{17.79}$$

while the number of clamping diodes per phase is

$$D_{clamp} = 2(N-2) \text{ but } (N-1)(N-2) \text{ if rated at switch voltage} \tag{17.80}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{17.81}$$

and the number of switches (and inverse parallel diodes) in each leg is

$$S_n = 2(N-1) \tag{17.82}$$

The basic three-level inverter (±½V_s, 0) is shown in figure 17.37, along with the basic three-level voltage from the leg output to centre tap of the capacitor string, R (neutral point). When switch T_1 is on, its complement T_1' is off, and visa versa. Similarly for the pair of switches T_2 and T_2'. Specifically T_1 and T_2 on give the output +½V_s, T_1' and T_2' on give the output -½V_s, and T_2 and T_1' on give the output 0. Essential to attaining these output levels, are the clamping diodes D_u and D_t. These two diodes clamp the outer switches to the capacitor string mid-point, which is half the dc rail voltage. In this way, no switch experiences a voltage in excess of half the dc rail voltage. Inner switches must be turned on (or off) before outer switches are turned on (or off).
The five-level inverter uses four capacitors, and eight switches in each inverter leg. A set of clamping diodes (three in total for each leg) clamp the complementary switches in each leg. The output is characterised by having five levels, ±½V_s, ±¼ V_s, and zero. Some of the clamping diodes experience voltages in excess of that experienced by the main switches. Series connection of some of the clamping diodes avoids this limitation, but at the expense of increasing the number of clamping diodes from 2×(*N*-2) to (*N*-1)×(*N*-2) per phase. Thus, depending on the diode position in the structure, two diodes have blocking requirements of

$$V_{RB} = \frac{N-1-k}{N-1} V_s \tag{17.83}$$

where $1 \le k \le N\text{-}2$. These diodes require series connection of diodes, if all devices in the structure are to support $V_s/(N\text{-}1)$. For $N > 2$, capacitor imbalance occurs at high modulation indices.
The general output voltage, to the centre of the capacitor string is given by

$$V_{an} = \frac{V_s}{N-1}(T_1 + T_2 + \ldots \ldots + T_{N-1} - \tfrac{1}{2}(N-1)) \tag{17.84}$$

Common to all diode clamped inverter, each phase leg is identical in structure, and all legs share a common dc link capacitor string.
Table 17.5 in combination with the six parts of figure 17.38, show the conducting devices for the six different output voltage and current combinations of the NPC inverter leg. The commercial inverter,

HVDC Light, uses the NPC structure in figure 17.37, but uses extensive series connection of devices to achieve a high dc link voltage. The main problem in increasing the number of output voltage levels, other than increased circuit complexity, is voltage balancing the dc link series connected capacitors at higher modulation levels, *M>½(N-1)*. This capacitor voltage balancing problem can be avoided when two multilevel inverters are used in an ac-dc-ac back to back converter arrangement, where the link capacitors are common to both converters.

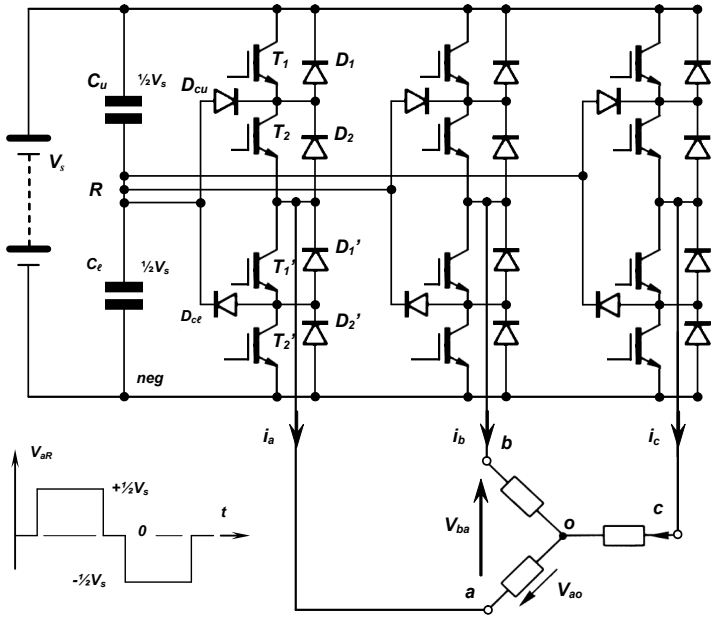


Figure 17.37. *Three-phase, voltage-source, three-level, diode-clamped (NPC) bridge inverter.*

Table 17.5: Conduction paths in the diode clamped three-level inverter

V_{out}	On switches	Output current and path + i_L		Output current and path - i_L		Active clamping diodes
½ V_s	T_1 T_2	T_1 T_2	Fig 17.38a	D_1 D_2	Fig 17.38d	none
0	T_1' T_2	D_{cu} T_2	Fig 17.38b	T_1' D_{ct}	Fig 17.38e	D_{cu} D_{ct}
-½ V_s	T_1' T_2'	D_1' D_2'	Fig 17.38c	T_1' T_2'	Fig 17.38f	none

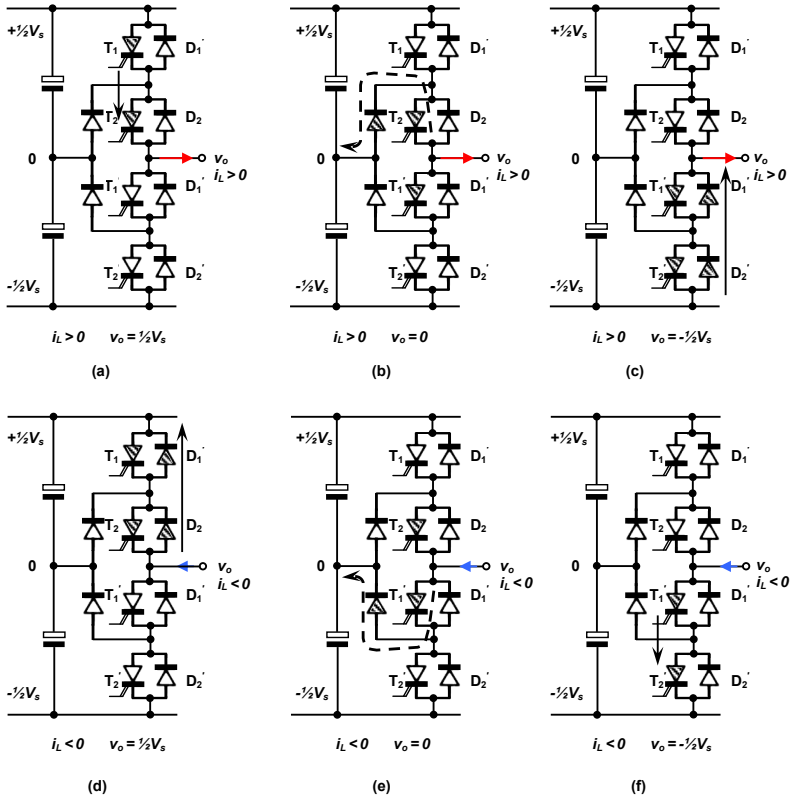


Figure 17.38. *The six output voltage and current combinations for the NPC bridge inverter: (a), (b), (c) output current $i_L > 0$; and (d), (e), (f) output current $i_L < 0$.*

17.3.2 Flying capacitor multilevel inverter

One leg of a fly-capacitor clamped five-level voltage source inverter is shown in figure 17.39b, where capacitors are used to clamp the switch voltages to ¼V_s. The available output voltages are ±½V_s, ±¼V_s, and 0, where the output is connected to the dc link (V_s and 0) indirectly via capacitors. Figure 17.39 shows that in general, switches T_n and T_{n+1} connect to capacitor C_n. The configuration offers more usable switch states than the clamped diode inverter, and this redundancy allows better, flexible control of capacitor voltages. For example, Table 17.5 shows that there are six states for obtaining 0V output, and four states for each of ±¼V_s. The output states ±½V_s do not involve the capacitors, hence they offer no redundant states. The basic switch restriction is that only one complementary switch (for example, T_4 or T_4') is on at any time, so as to prevent shorting of a flying capacitor (e.g., T_4 and T_4' would short C_3).
The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{17.85}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{17.86}$$

The number of capacitors required, which is dependent of the number of phase, is for each phase

$$N_{cap} = ½(N-1)(N-2) \tag{17.87}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{17.88}$$

and the number of switches in each leg is

$$S_n = 2(N-1) \tag{17.89}$$

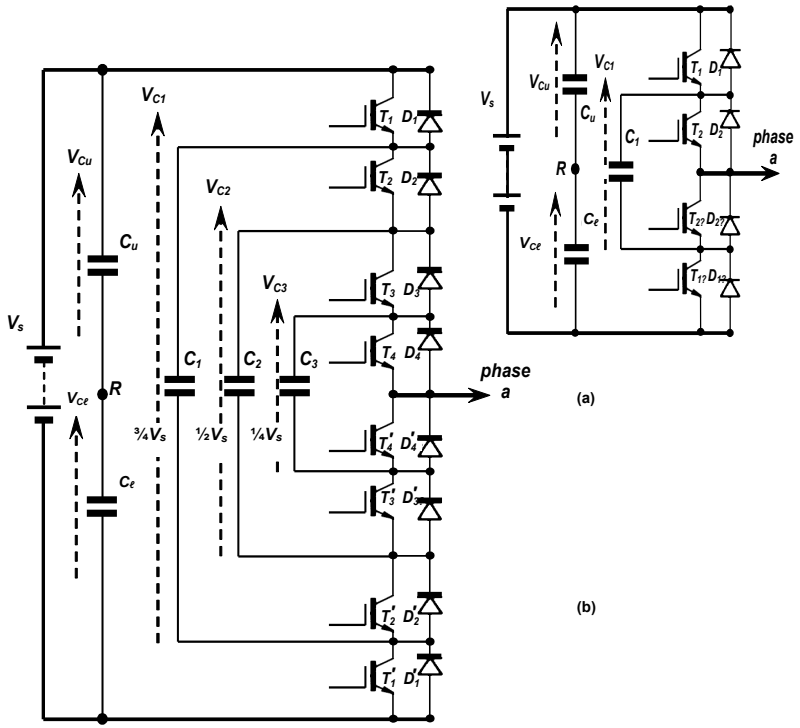


Figure 17.39. *One leg of a voltage-source:*
(a) three-level and (b) five-level, flying capacitor clamped bridge inverter.

Table 17.6: Five-level flying-capacitor inverter output states (phase A to R)

mode	V_{AR}	switch states				capacitors			paths
		T_1	T_2	T_3	T_4	C_1	C_2	C_3	
1	½V_s	1	1	1	1	=	=	=	½V_s
2 N-1 states	¼V_s	1	1	1	0	=	=	+	½V_s -V_{C3}
		1	1	0	1	=	+	-	½V_s -V_{C2}+V_{C3}
		1	0	1	1	+	-	=	½V_s-V_{C1}+V_{C2}
		0	1	1	1	-	=	=	-½V_s+V_{C1}
3 N^2-4N+1 states	0	1	1	0	0	=	+	=	½V_s -V_{C2}
		1	0	1	0	+	-	+	½V_s-V_{C1}+V_{C2} -V_{C3}
		0	1	1	0	-	=	+	-½V_s+V_{C1}-V_{C3}
		1	0	0	1	+	=	-	½V_s-V_{C1}+-V_{C3}
		0	1	0	1	-	+	-	-½V_s+V_{C1}-V_{C2}+V_{C3}
		0	0	1	1	=	-	=	-½V_s +V_{C2}
4 N-1 states	-¼V_s	1	0	0	0	+	=	=	½V_s-V_{C1}
		0	1	0	0	-	+	=	-½V_s+V_{C1}-V_{C2}
		0	0	1	0	=	-	+	-½V_s -V_{C2} -V_{C3}
		0	0	0	1	=	=	-	-½V_s +V_{C3}
5	-½V_s	0	0	0	0	=	=	=	-½V_s

The current output paths in Table 17.6 are made up by the series (and parallel) connection of the flying capacitors through the turn-on of the appropriate switches. Capacitors shown as negative are discharging in the formed path, while those shown as positive are charging. Use of the shown redundant states allows control to maintain the necessary voltage level on all the flying capacitors, while providing the desired output voltages.
A feature of the flying capacitor multilevel inverter is its ride through capability due to the large capacitance used. On the other hand, the capacitors have a high voltage rating and suffer from high current ripple, since they conduct the full load current when connected into an active output voltage state. Capacitor initial charging is also problematic, especially given the capacitors for each leg, and between the different legs, are independent.

If all the flying capacitors are voltage rated at the switch voltage level, then C_2 comprises two series connect capacitors and C_3 comprises three series capacitors, and all the same voltage rating as C_1.

17.3.3 Cascaded H-bridge multilevel inverter

The *N*-level cascaded H-bridge, multilevel inverter comprises ½(*N*-1) series connected single-phase H-bridges per phase, for which each H-bridge has its own isolated dc voltage source. For each bridge, as shown in table 17.7, three output voltages are possible, $\pm V_s$, and zero, giving a total number of states of $3^{½(N-1)}$, where *N* is odd. Figure 17.40 shows one phase of a seven-level cascaded H-bridge inverter.
The cascaded H-bridge multilevel inverter is based on multiple two level inverter outputs (each H-bridge), with the output of each phase shifted. Despite four diodes and switches, it achieves the greatest number of output voltage levels for the fewest switches.

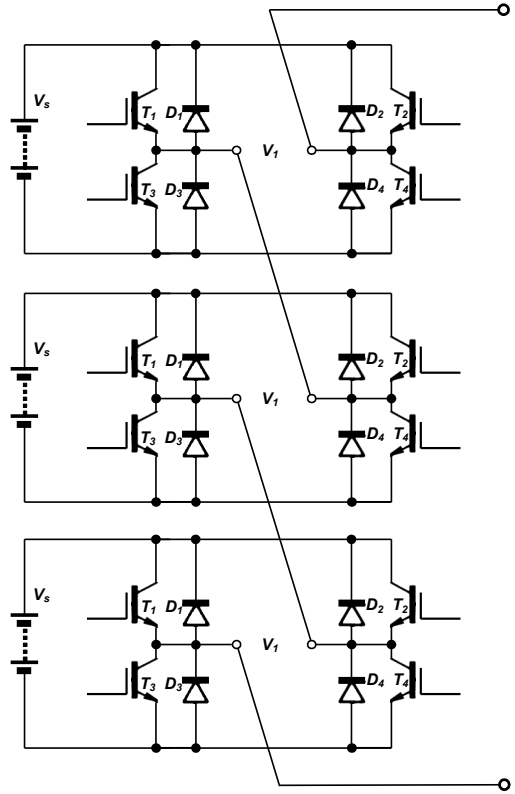


Figure 17.40. *One leg of a voltage-source, seven-level, cascaded H-bridge inverter.*

Table 17.7: Three output states of H-bridges and their current paths.

V_e	On switches	Bidirectional current paths	
		$+i_L$	$-i_L$
V_s	T_2 T_3	T_2 T_3	D_2 D_3
0	none	D_4 D_1	D_2 D_3
$-V_s$	T_1 T_4	T_1 T_4	D_2 D_3

Its main limitation lies in the need for isolated power sources for each H-bridge and for each phase, although for VA compensation, capacitors replace the dc voltage supplies, and the necessary capacitor energy is only to replace losses due to inverter losses. Its modular structure of identical H-bridges is a positive design feature.

The number of levels in the line-to-line voltage waveform will be

$$k = 2N - 1 \tag{17.90}$$

while the number of levels in the line to load neutral of a star (wye) load will be

$$p = 2k - 1 \tag{17.91}$$

The number of capacitors or isolated supplies required per phase is

$$N_{cap} = ½(N - 1) \tag{17.92}$$

The number of possible switch states is

$$n_{states} = N^{phases} \tag{17.93}$$

and the number of switches in each leg is

$$S_n = 2(N - 1) \tag{17.94}$$

17.3.4 Capacitor clamped modular multilevel M2C inverter

The capacitor-clamped modular multilevel inverter has several advantages compared to conventional multilevel inverters, such as: modular construction; can be extended to any number levels; capacitor voltage balance is attainable for any number of voltage levels; for a large number of voltage levels extremely low total harmonic distortion can be achieved without the need for filters. In addition, to reduced voltage stress on switching device *dv/dt*; and it has failure management capability in the case of device failures.

Figure 17.41 shows one cell of a capacitor-clamped multilevel converter, when the switching device S_m is turned on and S_c is turned off, the voltage $V_o = 0$; when the switching device S_m is turned off and S_c is turned on, the voltage $V_o = V_{dc}$. Table 17.8 and figure 17.41b summarizes the switch states of a cell shown in Fig. 17.41 and their influence in capacitor voltage. Switches S_m and S_c are complementary, when any one of them is on.

Figure 17.42 shows one-phase of the three-level capacitor-clamped inverter in which each voltage level can be synthesized by turning four switching devices simultaneously; in each instant two switches must belong to (S_{y1}, S_{y2}, S_{y3} and S_{y4}) and the remaining two from auxiliary switches (S_{x1}, S_{x2}, S_{x3} and S_{x4}). There are four complementary switch pairs in each phase, turning on one of the pair switches will excluded the other from being turned on. The four complementary switches are (S_{y1}, S_{x1}), (S_{y2}, S_{x2}), (S_{y3}, S_{x3}) and (S_{y4}, S_{x4}). For a dc bus of V_{dc}, the voltage across each cell capacitor is $½V_{dc}$ and each switching device voltage stress is limited to one capacitor voltage. For an *n*-level converter, the voltage across each capacitor and switching device is limited to $V_{dc}/(n-1)$ while the number of switching devices (IGBT plus free wheeling diode) required per phase is doubled that for multipoint clamped converters. The number of capacitors required for three-phases is *6n-6* (*2n-2* per phase), while no clamping diodes are required. To explain how the multilevel waveform voltage is synthesized, the supply mid point is assumed the output voltage reference. Using the three-level converter circuit shown in Figure 17.42 as an example, there are six switching combinations to synthesize three-level voltages between *x* and *o*.

1. For voltage level $V_{xo} = ½V_{dc}$, turn on all the upper main switches (S_{y1} and S_{y2}) and all the lower auxiliary switches (S_{x3} and S_{x4}).
2. For voltage level $V_{xo} = 0$, there are four different switch combinations:
   a) turn on S_{y1}, S_{y3}, S_{x2} and S_{x4}
   b) turn on S_{y2}, S_{y3}, S_{x1} and S_{x4}
   c) turn on S_{y2}, S_{y4}, S_{x1} and S_{x3}
   d) turn on S_{y1}, S_{y4}, S_{x2} and S_{x3}
3. For voltage level $V_{xo} = -½V_{dc}$, turn on all the upper auxiliary switches (S_{x1} and S_{x2}) and all the lower main switches (S_{y3} and S_{x4}).

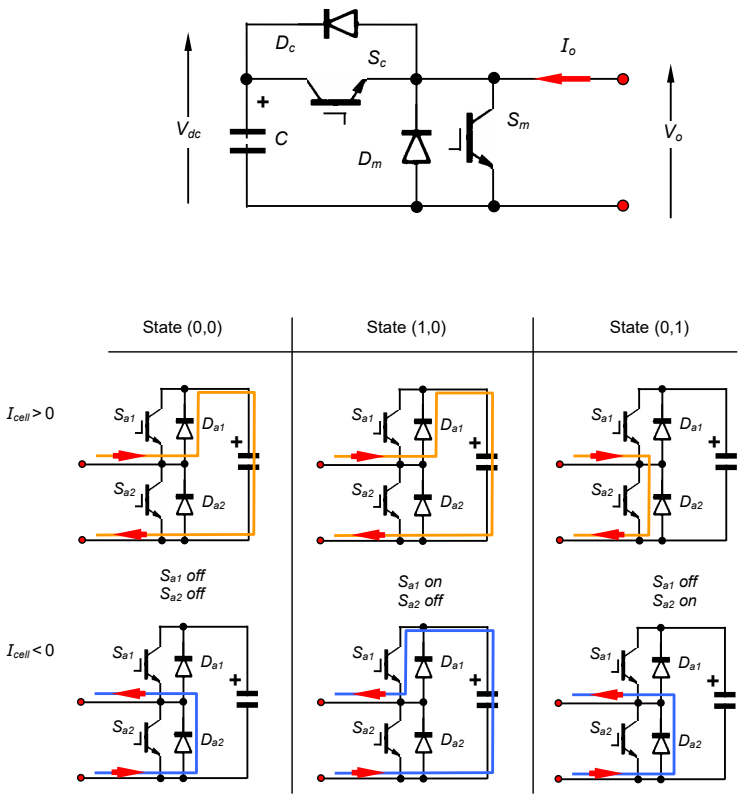


Figure 17.41. *Structure of one cell in capacitor-clamped multilevel converter and its current direction dependant conduction states.*

Table 17.8: Switch states of one cell

S_m	S_c	V_o	Current direction	Power path	Capacitor state
ON	OFF	0	$i_o > 0$	S_m	unchanged
ON	OFF	0	$i_o < 0$	D_m	unchanged
OFF	ON	V_{dc}	$i_o > 0$	D_c	charging
OFF	ON	V_{dc}	$i_o < 0$	S_c	discharging

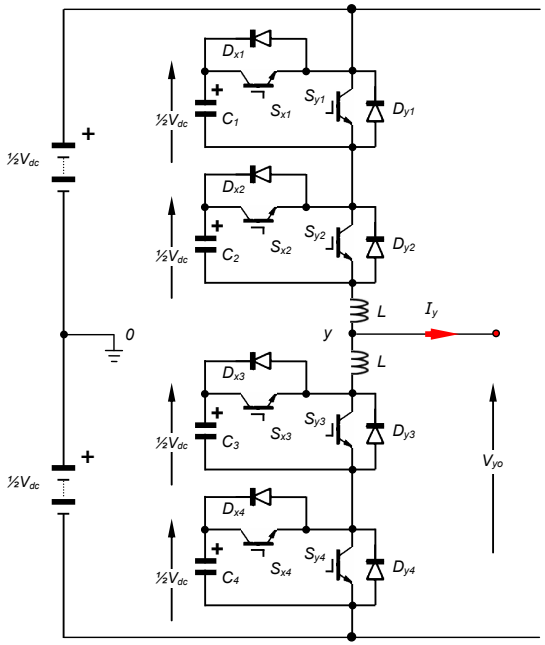


Figure 17.42. *Schematic for one-leg of a three-level capacitor-clamped multilevel (M2C) inverter.*

Table 17.9 lists the voltage levels and their corresponding switch states. State condition 1 means the switch is on, and 0 means the switch is off. In order to maintain equal voltage stressing on the switching devices, the voltage across each cell capacitor must be maintained at $½V_{dc}$.

Table 17.9: Switching combinations for three-level capacitor-clamped M2C converter

output voltage V_{xo}	switch states								
	S_{y1}	S_{y2}	S_{y3}	S_{y4}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
$½V_{dc}$	1	1	0	0	0	0	1	1	
0	1	0	1	0	0	1	0	1	(a)
	0	1	1	0	1	0	0	1	(b)
	0	1	0	1	1	0	1	0	(c)
	1	0	0	1	0	1	1	0	(d)
$½V_{dc}$	0	0	1	1	1	1	0	0	

A consequence of capacitor voltage balancing and PWM operation is a significant dc current component in each leg that contributes to an increase in switch losses.

Multilevel topology comparison

A comparison between the three basic multilevel inverters is possible from the numerical summary of component numbers for each inverter, as in Table 17.10.

The diode clamped inverter requires many clamping diodes; the flying capacitor inverter requires many independent capacitors; while the cascaded inverter requires many isolated dc voltage power supplies.

Table 17.10: Multilevel inverter component count, per phase

Inverter type * either /or	levels			switches & // diodes	diodes clamping	flying capacitors	level capacitors	isolated supplies	Outer hex redundant states
	V_{A-0V}	V_{A-B}	V_{A-N}						
diode clamped	*N*	*2N-1*	*4N-3*	*2(N-1)*	*(N-1)(N-2)*	0	*(N-1)*	1	0
flying capacitor	*N*	*2N-1*	*4N-3*	*2(N-1)*	0	*½(N-1)(N-2)*	*(N-1)*	1	yes
cascade	*N (odd)*	*2N-1*	*4N-3*	*2(N-1)*	0	0	*½ (N-1)**	*½(N-1)**	n/a
capacitor clamped	*N*	*2N-1*	*4N-3*	*4(N-1)*	0	0	*2(N-1)*	1	yes

17.3.5 PWM for multilevel inverters

Two basic approaches can be used to generate the necessary pwm signals for multilevel inverters. Each approach is based on the extension of a two level equivalent.

- Modulating waveform comparison with offset triangular carriers
- Space vector modulation based on a rotating vector in multilevel space

17.3.4i - Multiple offset triangular carriers

Various sinusoidal pwm techniques were considered in sections 17.1.3v and 17.1.3vi of this chapter. Figure 17.43 shows how a triangular carrier is associate with each complementary switch pair, four carriers (*N*-1) for the five-level inverter as illustrated. The parts of figure 17.43 show how the four individual carriers can be displaced with respect to one another. The figure also shows how triplen injection is incorporated. The appropriate five-level switch states, as in tables 17.4 to 17.6, can be used to decode the necessary switching sequences. To minimise losses, switching is restricted to only occur between adjacent levels.

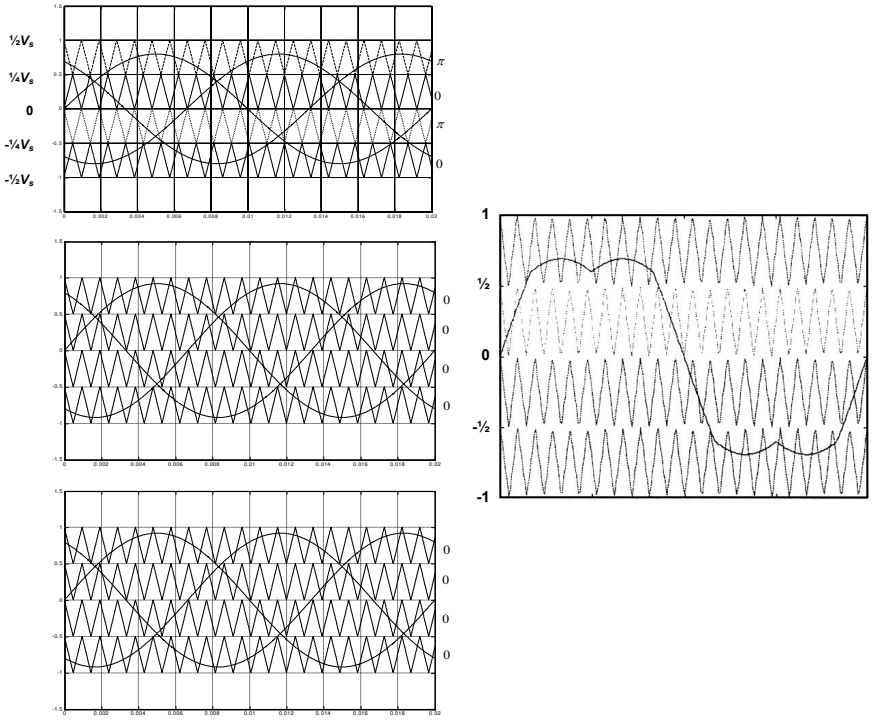


Figure 17.43. *Multi-carrier based pwm generation for a voltage-source, 5-level, inverter.*

17.3.4ii - Multilevel rotating voltage space vector

Space vector modulation for the two-level inverter was considered in section 17.1.3vi of this chapter. The basic hexagon shape for two levels is extended to higher levels as shown in figure 17.44, for three levels. The number of triangles, vectors, and states increases rapidly as the level number increases.

Table 17.11: Properties of *N*-level vector spaces

levels	states	triangles	vectors	vectors in each hexagon
N	N^3	$6(N-1)^2$	$3N(N-1)+1$	
2	8	6	7	(1+6)
3	27	24	19	(1+6)+12
5	125	96	61	(1+6)+12+18+24

From Table 17.11, the states for the two and three level inverters can be specified as follows.

The 2-level inverter

The zero state matrix is

$$\begin{bmatrix} 000 & 111 \end{bmatrix}$$

The first and only hexagon is shown in figure 17.24a.

$$\begin{bmatrix} 100 & 110 & 010 & 011 & 001 & 101 \end{bmatrix}$$

The three level inverter

The zero state matrix is

$$\begin{bmatrix} 000 & 111 & 222 \end{bmatrix}$$

The first hexagon matrix is

$$\begin{bmatrix} 100 & 110 & 010 & 011 & 001 & 101 \\ 211 & 221 & 121 & 122 & 112 & 212 \end{bmatrix}$$

The second hexagon matrix is

$$\begin{bmatrix} 200 & 210 & 220 & 120 & 020 & 021 & 022 & 012 & 002 & 102 & 202 & 201 \end{bmatrix}$$

These pole states are shown figure 17.44.

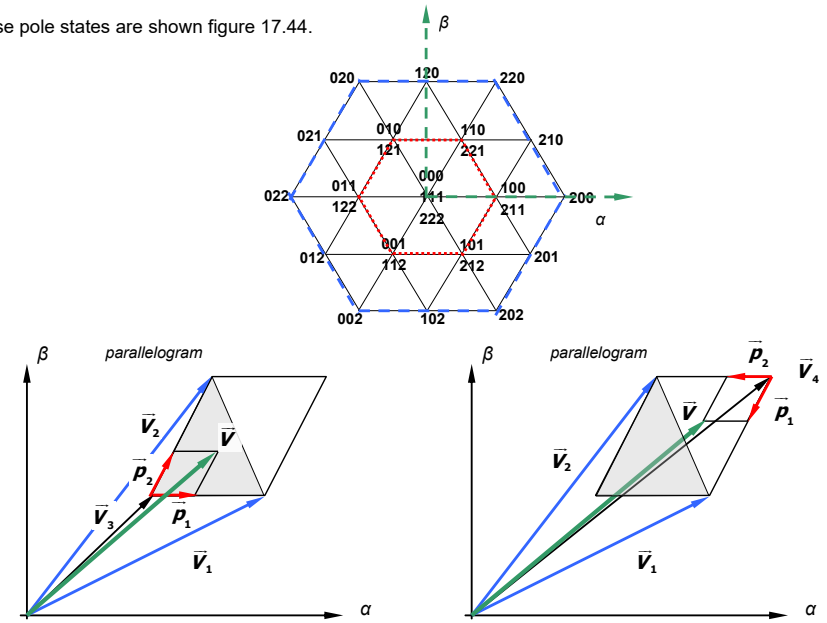


Figure 17.44. *Rotating voltage space vector approached applied to three phases of a voltage-source three-level, inverter and decomposition of the vector in a given parallelogram.*

A '0' represents the minimum voltage obtainable from the multilevel converter and *N-1* represents the maximum value. For example, in a two-level converter, '0' is equivalent to 0V and '1' is equivalent to V_s, where V_s is the converter DC link voltage. In a three-level converter '0' is equivalent to $-½V_s$, '1' is equivalent to 0 V, and '2' is equivalent to $½V_s$ where V_s is the dc link voltage of the multilevel converter.
When the rotating vector is drawn in the vector space, it is decomposed into vectors bordering the triangle it lies in. When operating in the outer hexagon, the vectors states used in the inner most hexagon mean that that level of the converter is operating with a six-step quasi-square output voltage waveform, to which is added a modulated square waveform for the next higher level.

Generally, the rotating vector can lay in one of two triangles of any parallelogram. Once the parallelogram has been uniquely decoded, for the triangle nearer the origin:

$$\begin{aligned} \vec{V} &= p_1\left(\vec{V}_1 - \vec{V}_3\right) + p_2\left(\vec{V}_2 - \vec{V}_3\right) + \vec{V}_3 = p_1\vec{V}_1 + p_2\vec{V}_2 + (1 - p_1 - p_2)\vec{V}_3 \\ &= \vec{p}_1 + \vec{p}_2 + \vec{V}_3 \end{aligned} \tag{17.95}$$

while for the triangle further from the origin:

$$\begin{aligned} \vec{V} &= p_1\left(\vec{V}_1 - \vec{V}_4\right) + p_2\left(\vec{V}_2 - \vec{V}_4\right) + \vec{V}_4 = p_1\vec{V}_1 + p_2\vec{V}_2 + (1 - p_1 - p_2)\vec{V}_4 \\ &= \vec{p}_1 + \vec{p}_2 + \vec{V}_4 \end{aligned} \tag{17.96}$$

where p_1 and p_2 are the relative duration lengths of the active vectors V_1 and V_2.
The zero vectors, V_3 and V_4, constitute the remaining time in the carrier period not assigned to the V_1 and V_2 associated duration components. The periods associated with p_1V_1 and p_2V_2 are distributed within the carrier period as for to level SVM in section 17.1.3vii-2.
Since SVM decomposes a single rotating vector into three identical components displaced by 120°, such a modulation strategy may not be applicable to any inverter used for FACTS type applications since phases may be unbalanced, distorted or phase shifted.

Multilevel converter advantages:

- Low THD and lower *dv/dt* than conventional two-level converters at the same switching frequency.
- Blocking voltage of each switch is clamped to a divided capacitor link voltage level.
- Lower common mode (CM) voltage, thus reduce insulation stresses. With sophisticated modulation methods, the CM voltage can be eliminated.
- Scalable to different power and voltage levels.
- Inherent reliability. If a multilevel converter component fails, the desired output voltage can still be produced because of module redundancy.

Multilevel converter disadvantages:

- Control becomes complex with increased number of levels.
- Multiple DC voltages are required, which are usually provided by capacitors.
- Balancing capacitor voltages is a challenge.
- Switching losses increase with an increase in the number of levels.
- Numerous clamping diodes and capacitors are required, therefore system costs increase.
- Switching device current ratings vary due to different conduction duty cycles.

17.4 Reversible dc link converters

Power inversion by phase angle control is attained with a fully controlled single-phase converter as discussed in section 14.2.3. Power regeneration is also possible with the fully controlled three-phase converter shown in figure 14.11. If a fully controlled converter supplies a dc machine, two-quadrant control is possible (QI and QII), motoring in one direction of rotation and generating in the other direction. Power regeneration into the supply is achieved by reversing the dc output voltage by controlling the converter phase delay angle. The converter current is uni-directional, that is, the converter output current cannot reverse.
The dual or double converter circuit in figure 17.45a and b will accommodate four-quadrant dc machine operation, where the circuit performs as two fully controlled converters in anti-parallel. Each converter is able to rectify and invert, but because of their inverse parallel connection, one converter (the positive converter P) operates in quadrants QI and QII, while the other (the negative converter N) operates in quadrants QIII and QIV, as shown in figure 17.46.
The two converters can be operated synchronously, called *simultaneous control* (circulating current mode) or independently where one is always blocking, called *independent control* (non-circulating current mode).

17.4.1 Independent control

Simultaneous converter control can be used if continuous load current can be guaranteed. Otherwise only one converter, depending on the quadrant, need operate at anyone time (the other is in a blocking state), as shown in figure 17.45a. No circulating currents arise due to possible mismatched N and P converter output voltages. The continuous current condition may be difficult to ensure at light load levels. Additional series armature inductance, L in figure 17.45a and b, helps with current smoothing and ensuring continuous machine current.

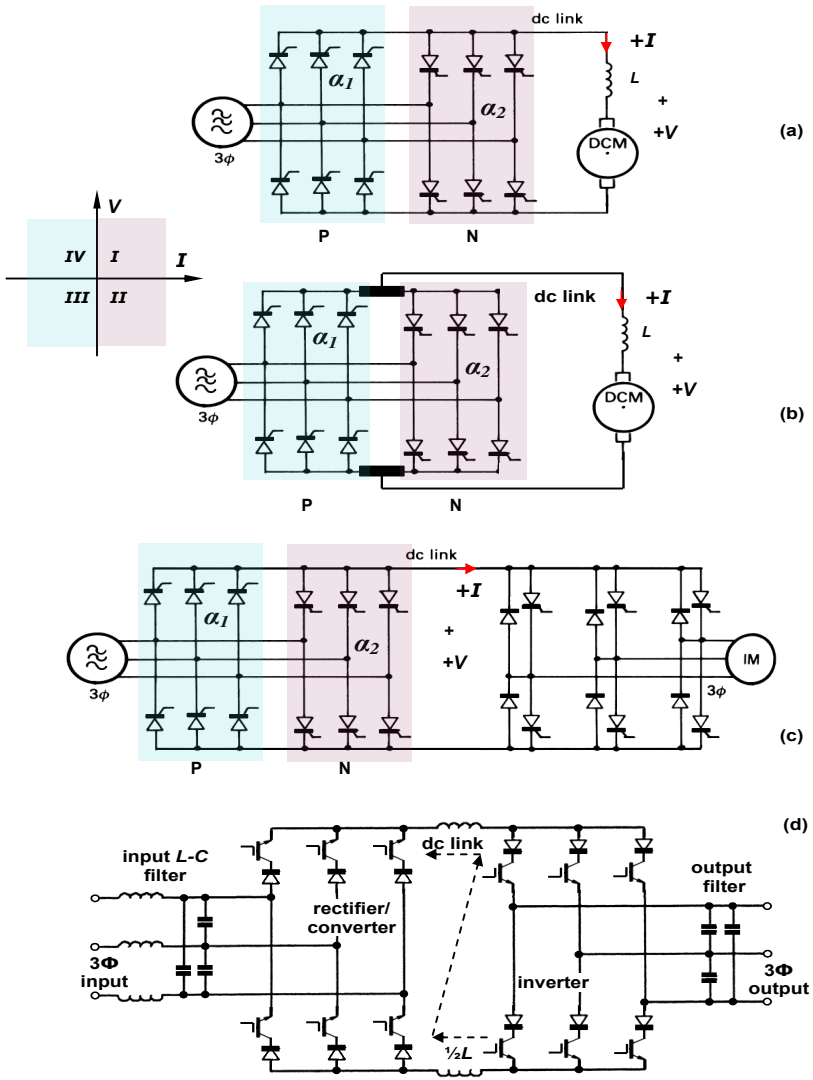


Figure 17.45. *Reversible converter allowing four-quadrant control of: (a) a dc machine with independent converters; (b) a dc machine with simultaneously controlled converters; and (c) voltage and (d) current fed induction machine.*

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I (rectification), with $0° \le \alpha_1 \le 90°$ for the positive converter P. The negative converter, N, is in the fully blocking state, with all thyristors turned off. Both V_o and I_o are positive, hence the average load power P_o is positive with power flowing from ac source to the load.
- The positive converter is put into the inverting mode with $90° \le \alpha_1 \le 180°$, (quadrant II) changing the average output voltage from positive to negative. V_o is negative and I_o is positive, hence the average load power P_o is negative with power flowing from the load circuit to the ac source.The machine current rapidly falls to zero. The machine rotational speed slows, the rate depending on the load inertia.
- After a dead time, the positive converter blocks and the negative converter N starts in a motor braking mode in quadrant II, with $0° \le \alpha_2 \le 90°$. The motor speed falls rapidly to zero.
- The second converter operates in quadrant III and rapidly accelerates the motor in the opposite direction, with $0° \le \alpha_2 \le 90°$. Both V_o and I_o are negative, hence the average load power P_o is positive with power flowing from ac source to the load.

Reversal back to the original direction commences with

- With converter P remaining off, converter N operates with $\alpha_2 > 90°$ in the inversion mode, quadrant IV. V_o is positive, I_o is negative hence the average load power P_o is negative. Power (hence energy) flows from the load circuit to the ac supply source.

The dead time before turning on the negative converter N is to ensure the positive converter P is fully off (and vice versa), otherwise the three-phase input voltage lines may short through the two converters. Such a current condition cannot be controlled with line-commutated thyristors. Operation is characterised by transitions from QI to QII to QIII for reversal, and transitions from QIII to QIV to QI for returning to the original direction of rotation. Transition between the two converters occur with dead times so that only one converter is ever activated.

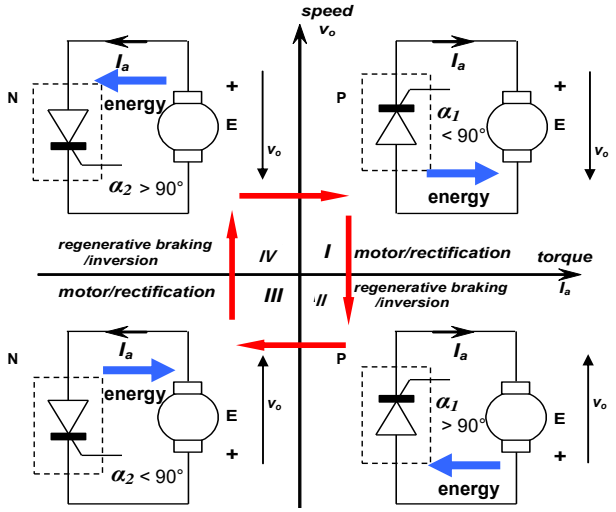


Figure 17.46. *Four quadrants of reversible converter operation.*

17.4.2 Simultaneous control

Simultaneous converter control, also called circulating current control, functions with both converters always in operation which gives a faster dynamic response than when the converters are used mutually exclusively. To avoid supply short circuits requires that the output voltage of both converters (rectifier V_r and inverter V_i) be the same in order to minimise circulating currents.

$$\begin{aligned} \bar{V}_r + \bar{V}_i &= 0 \\ V\cos\alpha_1 + V\cos\alpha_2 &= 0 \\ \cos\alpha_1 + \cos\alpha_2 &= 0 \\ \text{that is } \alpha_1 + \alpha_2 &= 180^\circ \end{aligned} \qquad (17.97)$$

Equation (17.97) implies that both converters operate with firing angles that sum to 180°. Each converter produces the opposite polarity average output voltage, which is cancelled by reversing the relative output connections. Under such conditions the load current can be maintained continuous. To minimize any circulating current due to ripple voltage produced by instantaneous voltage differences between the two converters, inductance L_r is usually inserted between each converter and the dc machine load, as shown in figure 17.45b. Adversely the cost and weight are increased, and the supply power factor and drive efficiency are decreased, compared to that obtained with independently controlled converters.

During interval $\frac{1}{6}\pi + \alpha_1$ to $\frac{1}{2}\pi + \alpha_1$, the line to line voltage v_{ab} appears across the output of converter 1 and v_{bc} appears across the output of converter 2

If v_{o1} and v_{o2} are the output voltages of converters 1 and 2 respectively, the instantaneous voltage across the circulating current limiting inductor L_r during the interval $\frac{1}{6}\pi + \alpha_1 \le \omega t \le \frac{1}{2}\pi + \alpha_1$ such that $\alpha_1 + \alpha_2 = \pi$, is given by

$$\begin{aligned} v_r &= v_{o1} + v_{o2} = v_{ab} - v_{bc} \\ v_r &= \sqrt{3}\,\sqrt{2}\,V\left[\sin\left(\omega t + \tfrac{1}{6}\pi\right) - \sin\left(\omega t - \tfrac{1}{2}\pi\right)\right] \\ v_r(\omega t) &= 3\sqrt{2}\,V\cos\left(\omega t - \tfrac{1}{6}\pi\right) \end{aligned} \qquad (17.98)$$

The circulating current is

$$\begin{aligned} i_r(t) &= \frac{1}{\omega L_r}\int_{\frac{\pi}{6}+\alpha_1}^{\omega t} v_r(\omega t)\, d\omega t \\ i_r(t) &= \frac{1}{\omega L_r}\int_{\frac{\pi}{6}+\alpha_1}^{\omega t} 3\sqrt{2}\,V\cos\left(\omega t - \tfrac{1}{6}\pi\right) d\omega t \\ \hat{i}_r &= \frac{3\sqrt{2}\,V}{\omega L_r} \end{aligned} \qquad (17.99)$$

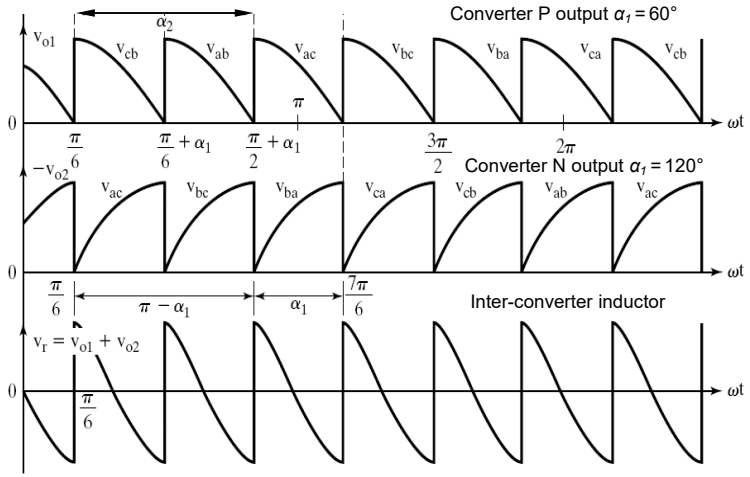


Figure 17.47. *Reversible converter output voltages and output ripple voltage*

A machine rotational direction change is affected by the following converter operating procedure.

- Initially the motor is operating in quadrant I for the rectifying, positive converter, with $0° \le \alpha_1 \le 90°$. The other converter is operating in the inverting mode with $90° \le \alpha_2 \le 180°$, such that $\alpha_1 + \alpha_2 = 180°$. The output voltage for both converters is the same, and the negative converter N carries only the circulating current.
- For rotational direction reversal, $\alpha_1 \ge 90°$ and $\alpha_2 \le 90°$, such that $\alpha_1 + \alpha_2 = 180°$. The armature back emf voltage now exceeds the converter output voltages, and current diverts to the negative converter N and the machine regeneratively brakes, operating in quadrant II. The current rapidly falls to zero and the positive converter P carries only the ac circulating current.
- The speed rapidly falls to zero, with $\alpha_1 = \alpha_2 = 90°$ giving zero output voltage, so as to control the armature current since the back emf is zero. Then with $\alpha_2 < 90°$ the machine rapidly accelerates in quadrant III, in the reverse direction to the original rotation.

For reversing the direction of rotation from Q III the operation sequence is QIII to QIV to QI. Since no converter dead time is introduced, a fast dynamic response can be attained. A small dc circulating current is deliberately maintained, that is greater in magnitude than the peak of the ac ripple current. The ac current can then flow continuously in both converters, both of which can operate in the continuous conduction mode without the need for continuous converter current reversal operation.

17.4.3 Inverter regeneration

The bridge freewheel diodes of a three-phase inverter restrict the dc rail or dc link voltage from reversing. The dual or double converter circuit in figure 17.45c will allow inversion with a three-phase voltage source inverter. One converter rectifies, the other converter inverts, functioning as a self-commutated inverter, transferring power from the dc link to the ac supply. Complete four-quadrant control of the three-phase ac machine on the inverter is achieved in conjunction with control of the dc to ac inverter. That is, motor reversal is achieved by effectively interchanging the pwm control signals associated with two phases. The real power flow back into the ac supply is controlled by the converter phase delay angle, while the reactive power flow is controlled by the voltage magnitude. The angle and voltage are not independent. In the case of a pwm controlled inverter fed ac machine, the ac to dc converter can be uncontrolled, using all diodes, since dc output voltage reversal is not utilised.

Figure 17.45d shows a fully reversible current controlled converter/inverter configuration, using self-commutating devices. The use of self-commutated switches (rather than mains commutated converter thyristors) offers the possibility to minimise the input current distortion and to reduce the inductor size hence improve the dynamic current response. The switch series diodes are essential since the shown IGBTs have no useable reverse blocking capability. The use of reverse blocking GCTs avoids the need for the series blocking diodes, which reduces the on-state voltage losses but increases gate drive complexity and power rating. Series connection of devices is necessary above a few kV, and above 1 MVA the GCT dominates.

17.5 Standby inverters and uninterruptible power supplies

Standby inverters and uninterruptible power supplies (UPS's) provide a 50/60 Hz supply in the event of an ac mains failure. A UPS must provide ac output such that mains failure is undetected by the load. To achieve this, a UPS continually feeds the load from an inverter. A load that can tolerate a short interruption of the ac supply is fed from a *standby inverter* which becomes operational within 1-5 ms after the ac supply failure. In communications, computing, and automated production lines, UPS's are essential for even brownouts (V and f outwith bounds for reliable equipment operation), while in lighting and heating applications, standby inverters are used since a few missing ac cycles (due to a blackout - total interruption of the mains power) may be tolerated. In each power supply case, the alternative energy source is a standby dc battery. The UPS keeps the battery charged when the ac input is supplying the output power.

17.5.1 Single-phase UPS

A basic single-phase UPS is shown in figure 17.48. A key safety objective is to retain the supply neutral at both the supply input and the ac output, without resorting to any from of isolating transformer. Consequently, the input ac mains is half-wave rectified by diodes D_R^+ and D_R^-. Boost converters on the positive and negative groups ensure supply sinusoidal input current and unity power factor. The output H-bridge (T_1-T_4) uses pwm and feedback control to produce a fixed frequency and magnitude output (and ac mains phase synchronisation if required), which is filtered by an *L-C* filter. In the event of a loss of the ac supply, the backup batteries, V^+ and V^-, provide energy to the boost converters, hence to the output inverter. The battery backup voltage magnitude is much less than the ac supply magnitude and diodes, D_B^+ and D_B^-, isolate the batteries from the rectified ac supply voltage. The shown UPS has two basic limitations that manufactures strive to overt.

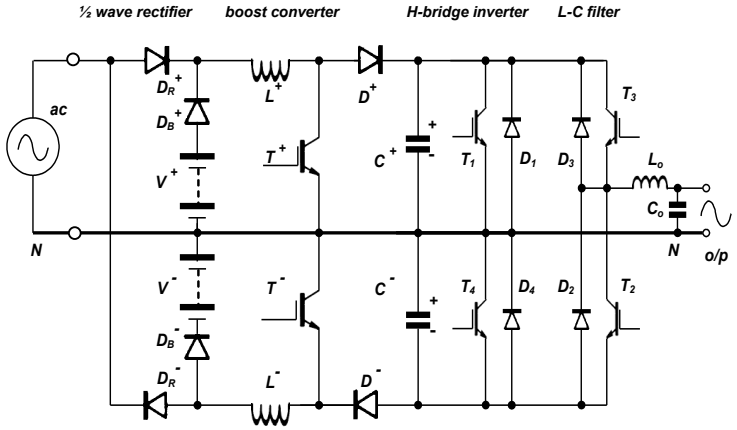
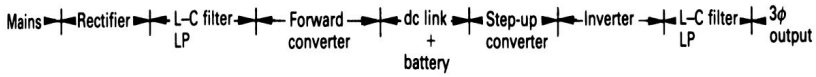


Figure 17.48. *Single-phase uninterruptible power supply.*

- If the battery is to be connected to neutral, then two batteries are necessary. Proprietary attempts using only one battery involve circuit complications and limitations. At best, with one battery, it is one forward biased diode voltage drop from neutral.
- Because the batteries supplies are not isolated during normal operation, during part of the mains cycle near zero voltage, the batteries alternately provide energy. This decreases their lifetime and necessitates more complicated trickle charge circuits. The input current is also distorted at the 0V crossover. Replacement of the blocking diodes D_B by switches involves complexity and battery backup operation requires detection and is not fail safe.



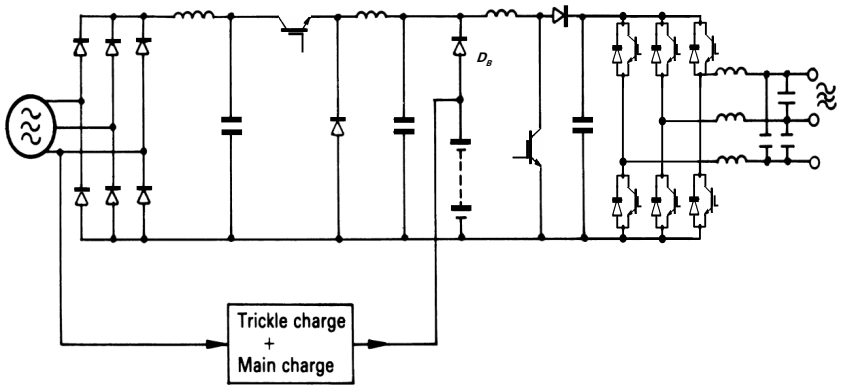


Figure 17.49. *Three-phase uninterruptible power supply.*

17.5.2 Three-phase UPS

Figure 17.49 shows a basic three-phase UPS, used up to a few tens of kilowatts. The ac supply is rectified and filtered. A forward converter controls the dc link voltage to just above the battery voltage level. This dc voltage is boosted to a dc level such that after inversion it provides the required output

voltage magnitude. If the input ac fails or droops, the dc link power is provided by the battery via diode D_B. The output inverter is usually operational in a pwm mode, which allows precise frequency control, voltage control, ac mains phase synchronisation, and minimisation of low frequency output harmonics. With pwm control minimal filtering is required, which minimises the filter weight, cost, size, and losses. A three-phase UPS can utilise third harmonic injection (17.1.4(iv)).
A three-phase boost input converter can be used to maintain sinusoidal ac supply input currents at unity power factor.

17.6 Power filters

Voltage sourcing converter outputs

Power *L-C* filters are used to reduce harmonics or ripple from voltage sourcing outputs, namely

- the rectifier output (dc filter)
- the inverter output (ac filter).

L-C low-pass, second-order filters are shown in figures 17.45, 17.48, and 17.49. In figure 17.49, the *L-C* smoothing filter at the rectifier output, filters the ac mains frequency components leaving dc. The same type of filter is used in the inverter output to filter pwm harmonics, leaving the relative low-frequency modulation frequency. In voltage sourcing outputs, the inductor is first (always in series) filter component, whether first order *L* only, second order *L-C*, or higher, *L-C-L*, etc.
The *L-C* filter fundamental cut-off frequency is dependent on *L, C,* and the load impedance Z_L

$$\frac{v_o}{v_i} = \frac{1}{1 + j\omega L\left(\frac{1}{Z_L} + j\omega C\right)} = \frac{1}{1 - \omega^2 LC + j\frac{\omega L}{Z_L}} \qquad (17.100)$$

The simplest design approach is to assume a no-load condition, $Z_L \to \infty$, whence the filter cut-off frequency is $f_o = 1/\left(2\pi\sqrt{LC}\right)$.

As a first pass, determine the necessary inductance as follows. Based on the assumption that all the source voltage is across the inductor because the capacitance tends to short the load (and maximum *di/dt* occurs at zero load voltage for a purely resistive load), then the inductance must allow the necessary maximum load *di/dt* at the maximum output frequency.

If the maximum fundamental current through the filter is

$$i(\omega t) = \sqrt{2}\hat{I}\sin\hat{\omega}t = \sqrt{2}\hat{I}\sin 2\pi\hat{f}\,t$$

where $\hat{f} \le f_o$

then the current *di/dt* controlled by the filter inductance is

$$\frac{di}{dt} = \sqrt{2}\hat{I}\,\hat{\omega}\cos\hat{\omega}t = 2\sqrt{2}\pi\hat{f}\,\hat{I}\cos 2\pi\hat{f}\,t$$

which has a maximum value at 0 radians, when cos $\omega t = 1$. That is, using $V = L\,di/dt$ rearranged

$$\hat{L} = \frac{\hat{V}}{di/dt} = \frac{\hat{V}}{\sqrt{2}\hat{I}\,\hat{\omega}} = \frac{\hat{V}}{2\sqrt{2}\pi\hat{f}\times\hat{I}} \qquad (17.101)$$

Then $f_o = 1/\left(2\pi\sqrt{LC}\right)$ is used to calculate the necessary capacitance.
Frequency components below f_o, including dc, are passed. Those components above f_o are attenuated by a second order fall-off in gain. Any frequency components inadvertently around the resonant frequency, f_o, will be amplified. For this reason, the filter may be damped with parallel connected *R-C* snubbers.

Other constraints on the filter *L*, may include output dynamic response and rate of rise of fault current.

Example 17.6: ***L-C filter design, for voltage sourcing converter output***

A 220V ±10% dc sourced H-bridge inverter, switching at 100kHz outputs 1Hz to 5kHz, 100A rms maximum. Design an *L-C* filter to give maximum attenuation of the 100kHz carrier frequency.

Solution

The maximum current, 100A rms, at maximum frequency, 5kHz, is given by

$$i\left(2\pi 5\text{kHz}\times t\right) = \sqrt{2}\times 100\text{A}\times\sin 2\pi 5\text{kHz}\times t$$

Differentiating leads to the maximum *di/dt* experienced by the series filter inductor, specifically

$$\sqrt{2}\hat{I}\,\hat{\omega} = 2\sqrt{2}\pi\hat{f}\,\hat{I}$$
$$= 2\sqrt{2}\pi \times 5\text{kHz} \times 100\text{A} = 4.44\text{A/}\mu\text{s}$$

Assuming the filter capacitor tends to short the load at 100kHz and zero load voltage occurs at maximum *di/dt*, the source voltage is impressed across the filter inductor. Rearranging $V = L di/dt$, gives

$$\hat{L} = \frac{\hat{V}}{2\sqrt{2}\pi\hat{f} \times \hat{I}}$$
$$= \frac{200\text{V}}{4.44\text{V/}\mu\text{s}} = 45\mu\text{H}$$

The maximum usable inductance is 45μH up to 100kHz, rated at 100A rms. These requirements imply using cores with an air gap to avoid saturation with a minimum volume. Amorphous strip C cores wound with copper foil are suitable. Use half the inductance in each output pole for pseudo s/c protection.

In spite of the expected filter high resonance *Q*, a filter cut-off frequency equal to the maximum output frequency of 5kHz can be used, provided output voltage feedback is used to compensate for the near resonance effects. Using a 5kHz cut-off frequency gives maximum attenuation of the 100kHz carrier. Using $f_o = 1/2\pi\sqrt{LC}$ gives

$$C = \frac{L}{(2\pi f_o)^2}$$
$$= \frac{45\mu\text{H}}{(2\pi 5\text{kHz})^2} = 45.6\text{nF} \approx 47\text{nF}$$

The capacitor requirements include low resistance, implying metallised polypropylene. The voltage rating is related to the maximum rms voltage associated with a 220V squarewave, which is 4×220/√2×π = 198V rms at 5kHz. Given modulation is used, 220V ac is conservative. A double metallised polypropylene capacitor should have an adequate *dv/dt* rating, hence 100kHz ripple current rating.

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Current sourcing converter outputs

In current sourcing outputs, as in figure 17.30, the filter capacitor is first (always in shunt) filter component, whether first order *C* only, second order *C*-*L*, or higher, *C*-*L*-*C*, etc. The shunt C capacitance is based on the maximum output voltage (*dv/dt*) requirement of the converter and $i = C\,dv/dt$.
Other constraints on the filter *C*, may include output dynamic response and rate of rise of fault voltage.

Reading list

See chapter 15 reading list.

Hart, D.W., *Introduction to Power Electronics,*
Prentice-Hall, Inc, 1994.

Mohan, N., *Power Electronics,* 3rd Edition,
Wiley International, 2003.

Problems

17.1. The inverter in figure 17.7 is supplied from a 340 V dc source. The load has a resistance of 10Ω and an inductance of 10mH. The basic operating frequency is 50 Hz, with three notches per half cycle giving half the maximum output, similar to that shown in figure 17.14.
Determine the load current waveform over the first two cycles and determine the power delivered to the load based on the current waveform of the final half cycle.

17.2. The inverter and load in problem 17.1 are controlled so as to eliminate the third and fifth harmonics in the output voltage.
Determine the load current waveform over the first two cycles and the power delivered to the load based on the current waveform of the last half cycle.

17.3. Output voltage harmonic reduction can be achieved by employing multiphase, selected notching modulation control on a three-phase bridge as discussed in 17.1.4. An output as in figure 17.15b with $\alpha_1 = 16.3°$ and $\beta_1 = 22.1°$ eliminates the 5th and 7th harmonics.
Determine the fundamental voltage output component and compare it with that of a square wave. Determine the output rms voltage.

17.4. With the aid of figure 17.12 determine the line-to-neutral and line-to-line output voltage of a dc to three-phase inverter employing 120° device conduction.
Calculate the interphase:
- i. mean half-cycle voltage
- ii. rms voltage
- iii. rms voltage of the fundamental.

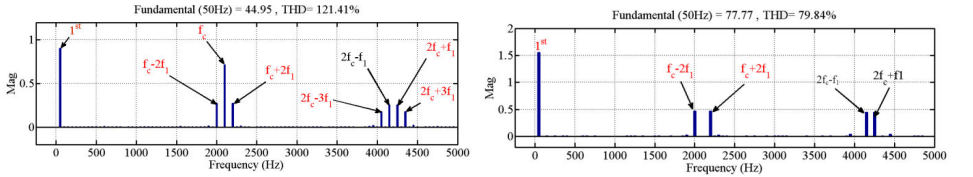
17.5. The three-phase inverter bridge in figure 17.4 has a 600V dc rail and a 10Ω per phase load. For 180° and 120° conduction calculate:
- i. the rms phase current
- ii. the power delivered to the load
- iii. the switch rms current.

[24.5 A, 18 kW, 17.3 A; 28.3 A, 24 kW, 14.15 A]

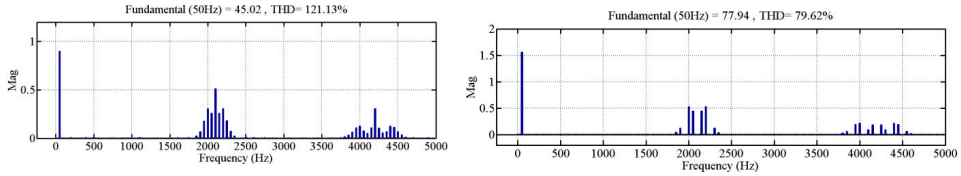
17.6 A single-phase square-wave inverter is supplied from a 340V dc source and the load is a 17Ω resistor. Determine switch average and rms current ratings. What power is delivered to the load?

17.7 A single-phase square-wave inverter is supplied from a 340V dc source and the series *R*-*L* load is a 20Ω resistor and *L*=20mH. Determine:
- i. an expression for the load current, hence the maximum switch current
- ii. rms load current
- iii. average and rms switch current
- iv. maximum switch voltage
- v. average source current, hence power delivered to the load
- vi. load current total harmonic distortion.

17.8. Compare the phase and line voltage spectrum of a 50Hz modulation process using 2.1kHz saw-tooth and triangular carriers.



Triangular carrier, 2.1kHz



Saw-tooth carrier, 2.1kHz